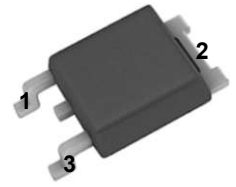
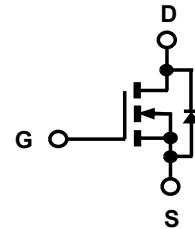


ICEK6NF65D N-Channel Enhancement Mode MOSFET

Features

- Low $r_{DS(on)}$
- Ultra Low Gate Charge
- High dv/dt capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems

Product Summary			
I_D	$T_A=25^\circ\text{C}$	6A	Max
$V_{(BR)DSS}$	$I_D=250\mu\text{A}$	650V	Min
$r_{DS(on)}$	$V_{GS}=10\text{V}$	0.51	Typ
Q_g	$V_{DS}=400\text{V}$	14nC	Typ



T0252

Standard Metal
Heatsink

1=Gate, 2=Drain,
3=Source.



Maximum ratings^a at $T_j=25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current ^b	I_D	$T_c=25^\circ\text{C}$	6	A
		$T_c=100^\circ\text{C}$	3.8	
Pulsed drain current ^b	$I_{D, \text{pulse}}$	$T_c=25^\circ\text{C}$	24	A
Avalanche energy, single pulse	E_{AS}	$L=75\text{mH}$, $V_{DD}=100\text{V}$, $I_D=0.9\text{A}$, $R_G=50\Omega$	30	mJ
Avalanche current, repetitive ^b	I_{AR}	limited by $T_{j\text{max}}$	0.9	A
MOSFET dv/dt ruggedness	dv/dt	$V_{DS}=480\text{V}$	50	V/ns
Reverse diode dv/dt ruggedness			50	
Gate source voltage	V_{GS}	Static	± 30	V
		AC ($f>1\text{Hz}$)		
Power dissipation	P_{tot}	$T_c=25^\circ\text{C}$	54.3	W
Operating and storage temperature	T_j, T_{stg}		-55 to +150	$^\circ\text{C}$

^a Preliminary data sheet - Specifications subject to change.

^b limited by $T_{j\text{max}}$

^c when mounted on 1-inch square 2oz copper-clad FR-4

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

Thermal characteristics

Thermal resistance, junction-case	R_{thJC}		-	-	2.3	°C/W
Thermal resistance, junction-ambient °	R_{thJA}	leaded	-	-	60	
Soldering temperature, wave soldering only allowed at leads	T_{sold}	1.6mm (0.063in.) from case for 10 s	-	-	260	°C

Electrical characteristics at $T_j=25^{\circ}\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.5	3.5	4.5	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=650V, V_{GS}=0V$	-	-	10	μA
Gate source leakage current	I_{GSS}	$V_{GS}=\pm 30V, V_{DS}=0V$	-	-	± 100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=4A$	-	0.51	0.6	Ω
Gate resistance	R_G	$f=1\text{ MHz}$, open drain	-	28	-	Ω

Dynamic characteristics

Input capacitance	C_{iss}	$V_{DS}=400V, V_{GS}=0V, f=1\text{ MHz}$	-	338	-	pF
Output capacitance	C_{oss}		-	13	-	
Reverse transfer capacitance	C_{rss}		-	5.5	-	
Turn-on delay time	$t_{d(on)}$	$V_{DS}=400V, V_{GS}=10V, I_D=4A, R_G=5\Omega$ (External)	-	52	-	ns
Rise time	t_r		-	8	-	
Turn-off delay time	$t_{d(off)}$		-	29	-	
Fall time	t_f		-	9	-	

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

Gate charge characteristics

Gate to source charge	Q_{gs}	$V_{DS}=400V, I_D=4A,$ $V_{GS}=0 \text{ to } 10V$	-	2	-	nC
Gate to drain charge	Q_{gd}		-	9	-	
Gate charge total	Q_g		-	14	-	

Reverse Diode

Continuous forward current	I_S	$V_{GS}=0V$	-	-	6	A
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_S=I_F$	-	1.3	-	V
Reverse recovery time	t_{rr}	$V_{RR}=400V, I_S=4A,$ $d_{iF}/d_t=100 \text{ A}/\mu\text{S}$	-	62	-	ns
Reverse recovery charge	Q_{rr}		-	0.33	-	μC
Peak reverse recovery current	I_{rm}		-	10	-	A

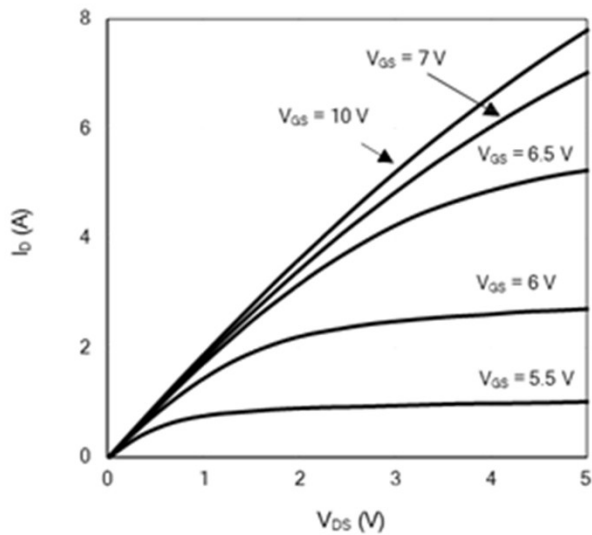


Figure 1: On-Region Characteristics

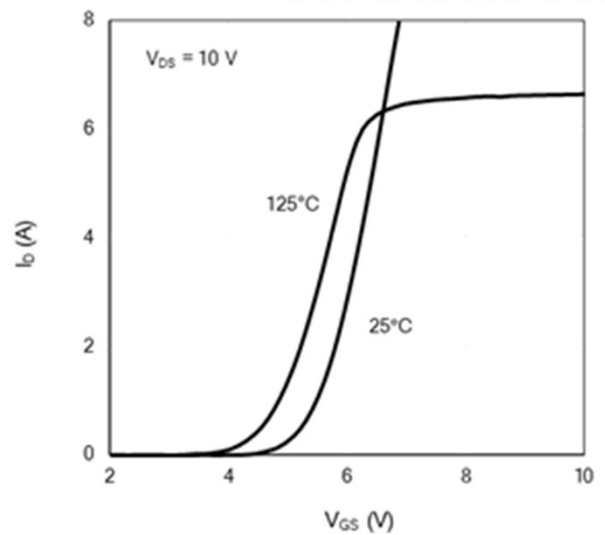


Figure 2: Transfer Characteristics

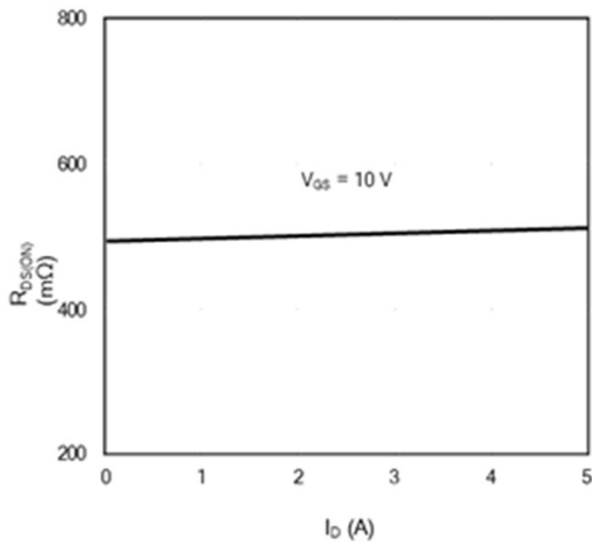


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

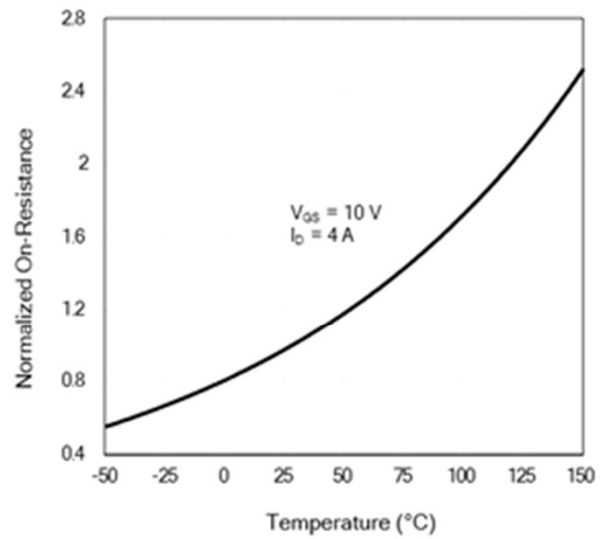


Figure 4: On-Resistance vs. Junction Temperature

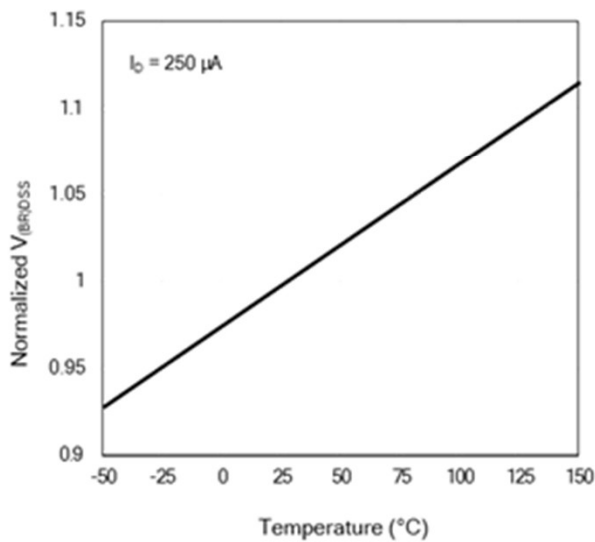


Figure 5: Breakdown Voltage vs. Junction Temperature

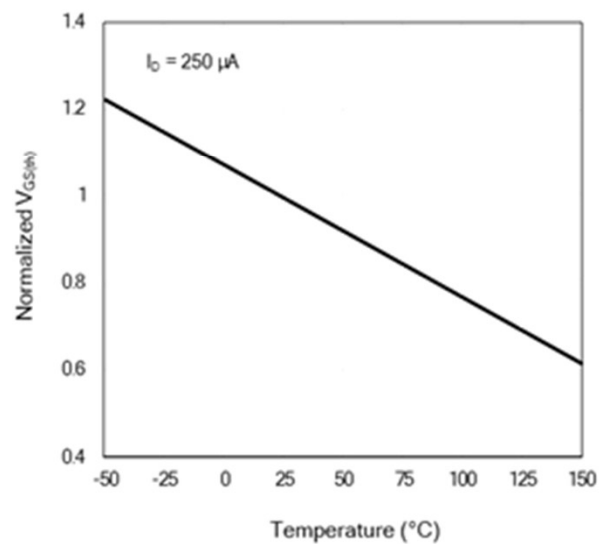


Figure 6: Threshold Voltage vs. Junction Temperature

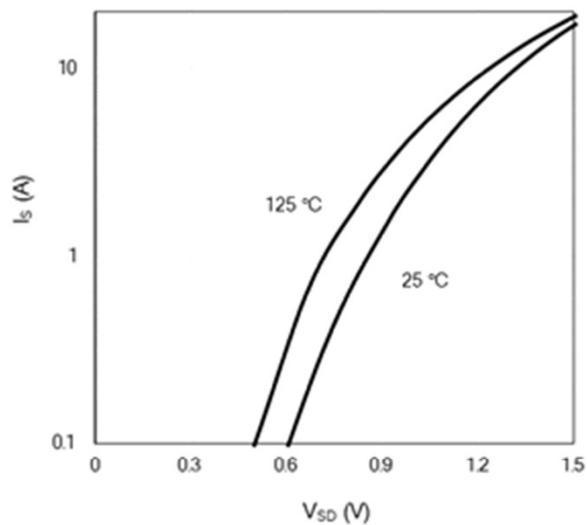


Figure 7: Body-Diode Characteristics

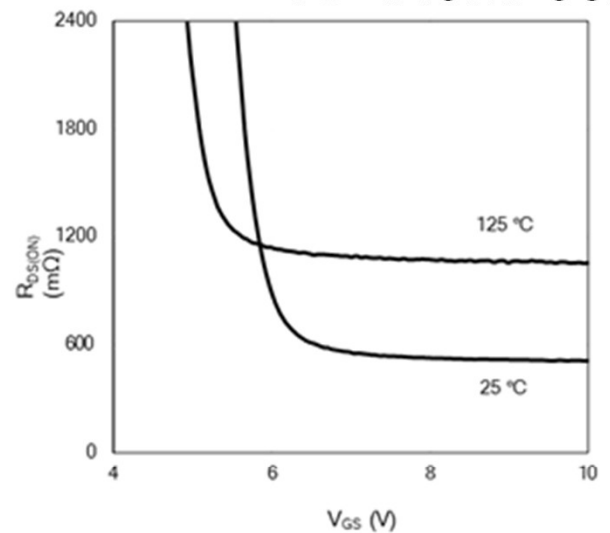


Figure 8: On-Resistance vs. Gate-Source Voltage

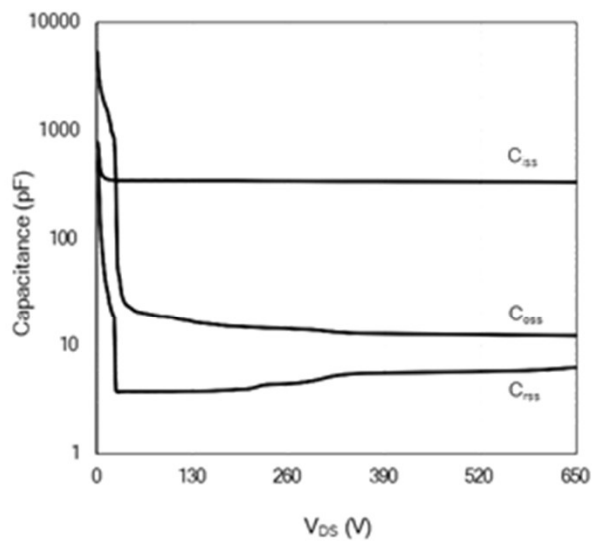


Figure 9: Capacitance Characteristics

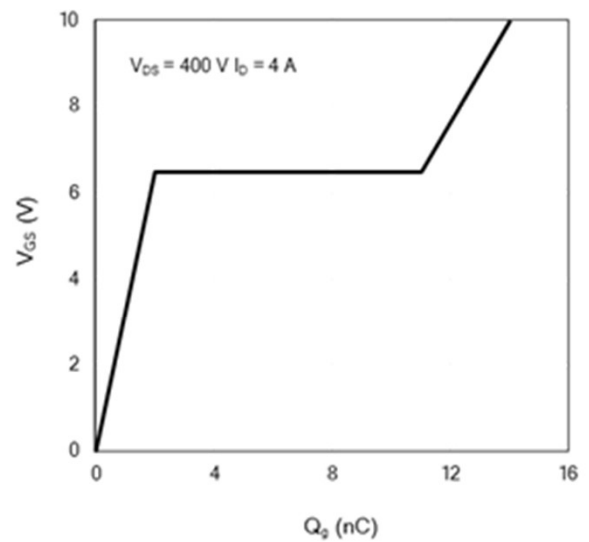


Figure 10: Gate-Charge Characteristics

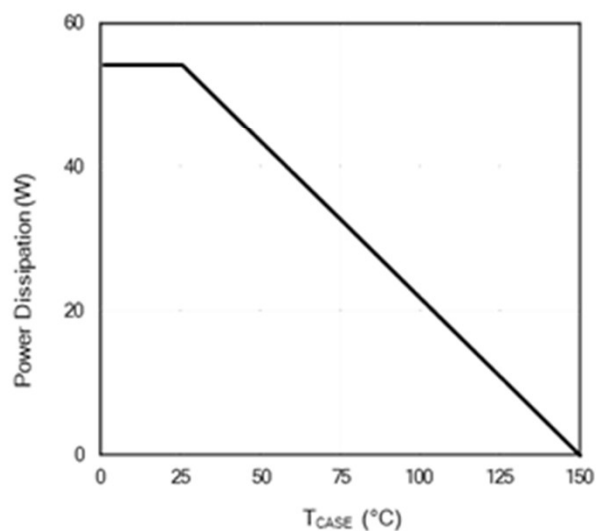


Figure 11: Power De-rating

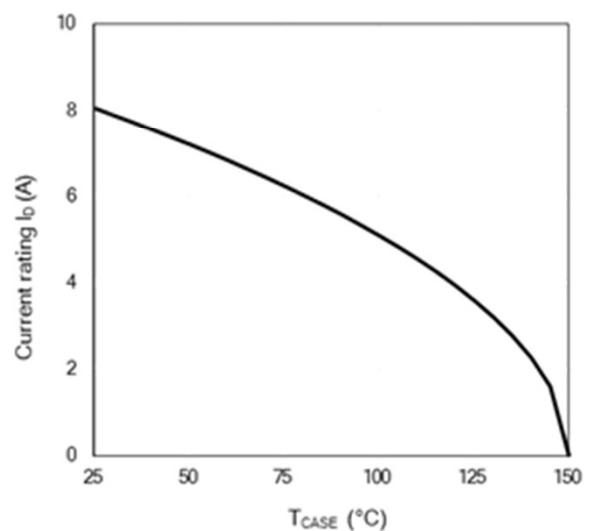


Figure 12: Current De-rating

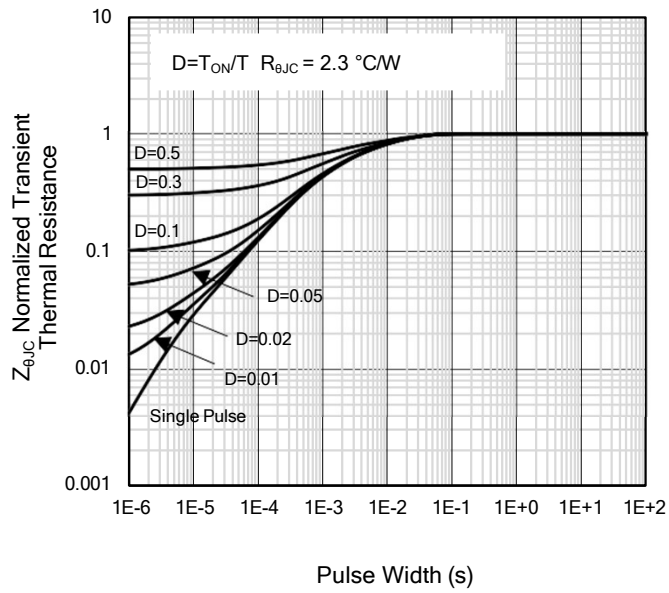


Figure 13: Normalized Maximum Transient Thermal Impedance

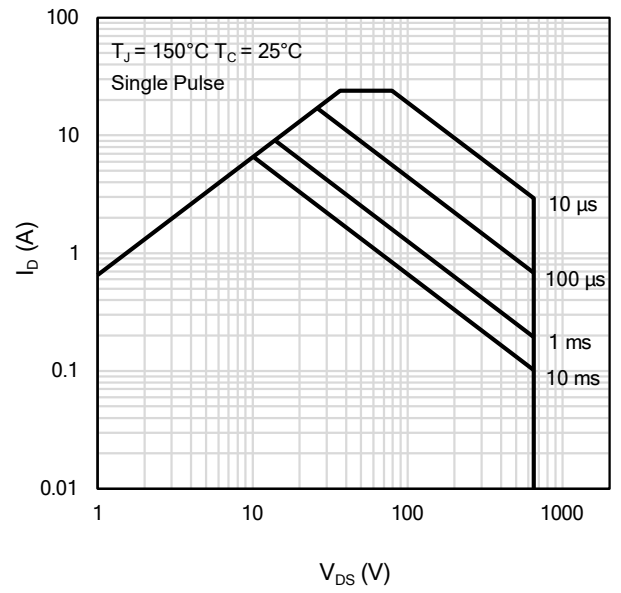
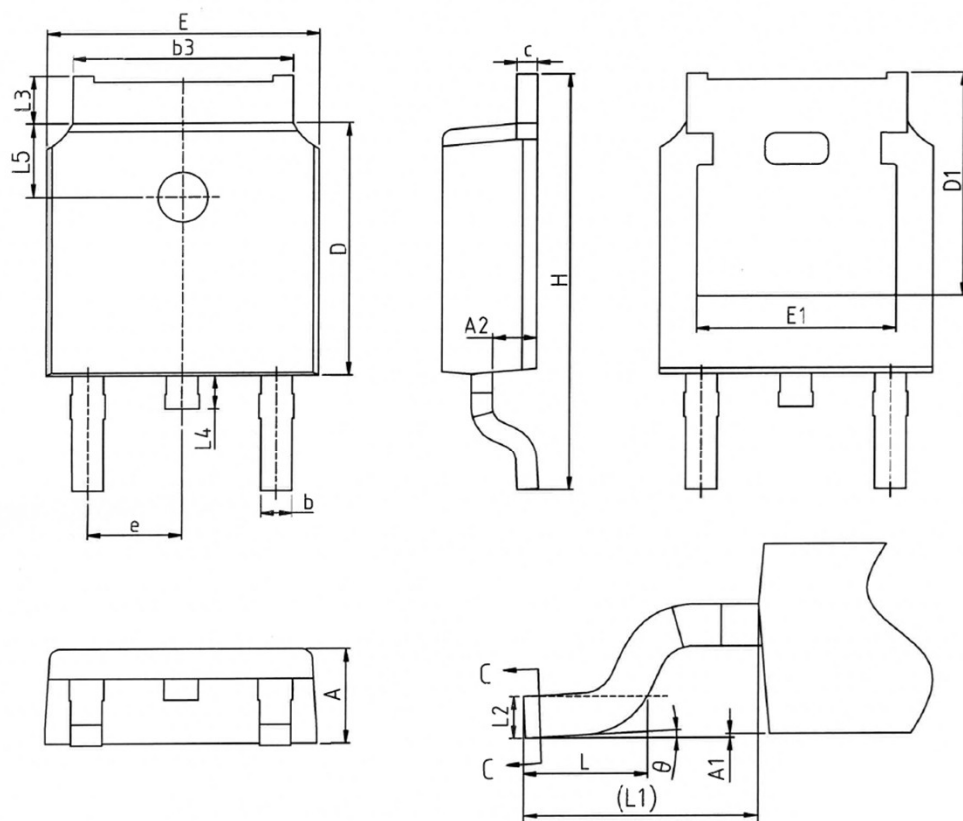


Figure 14: Maximum Forward Biased Safe Operating Area

Package Outline: TO252 (DPAK)



COMMON DIMENSIONS

SYMBOL	mm		
	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0.00	-	0.12
A2	0.97	1.07	1.17
b	0.68	0.78	0.90
b3	5.20	5.33	5.46
c	0.43	0.53	0.61
D	5.98	6.10	6.22
D1	5.30REF		
E	6.40	6.60	6.73
E1	4.63	-	-
e	2.286BSC		
H	9.40	10.10	10.50
L	1.38	1.50	1.75
L1	2.90REF		
L2	0.51BSC		
L3	0.88	-	1.28
L4	0.50	-	1.00
L5	1.65	1.80	1.95
θ	0°	-	8°

NOTES

1. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 AA, DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

Marking Information

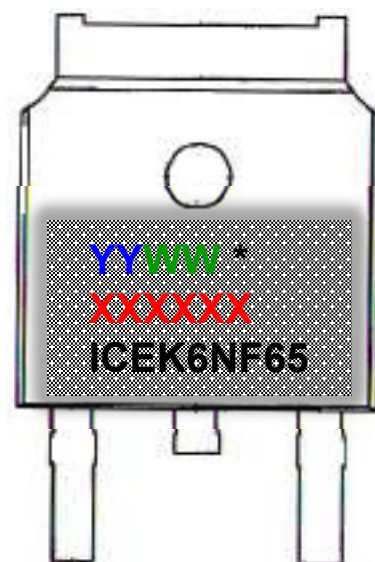
YY = Last two digits of the year

WW = Work week

***** = Site ID

XXXXXX = Lot ID

ICEK6NF65 = ICE is IceMOS logo and
K6NF65 is a designated device part
number



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