IceMOS Technology

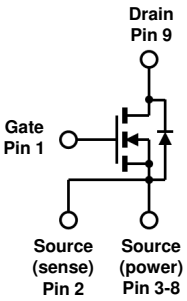
ICE8N60T

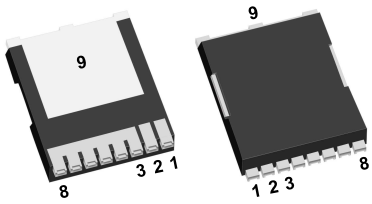
ICE8N60T N-Channel Enhancement Mode MOSFET

Product Summary			
I_D	T_A=25°C	8A	Max
$V_{(BR)DSS}$	I_D=250uA	600V	Min
$r_{DS(on)}$	V_{GS}=10V	0.43	Typ
Q_g	V_{DS}=480V	23nC	Typ

Features

- Low $r_{DS(on)}$
- Ultra Low Gate Charge
- High d*v*/d*t* capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems





TOLL

1=Gate, 2=Source(sense), 3-8 =Source (power), 9=Drain

RoHS COMPLIANT
RoHS (EU) 2015/863

CE

HALOGEN FREE

ICEMOS OWNS THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 to 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN & EUROPE.

Maximum ratings [a] at T_j=25°C, unless otherwise specified

Parameter	*Symbol*	*Conditions*	*Value*	*Unit*
Continuous drain current	I_D	T_c=25°C	8	A
		T_c=100°C	5	
Pulsed drain current	$I_{D,\ pulse}$	T_c=25°C	24	A
Avalanche energy, single pulse	E_{AS}	I_D=5.6A	156	mJ
Avalanche current, repetitive	I_{AR}	limited by $T_j$max	5.6	A
MOSFET d*v*/d*t* ruggedness	d*v*/d*t*	V_{DS}=480V, I_D=8A, T_j=125°C	50	V/ns
Gate source voltage	V_{GS}	Static	±20	V
		AC (*f*>1Hz)	±30	
Power dissipation	P_{tot}	T_c=25°C	95	W
Operating and storage temperature	T_j, T_{stg}		-55 to +150	°C

a limited by T_{jmax}

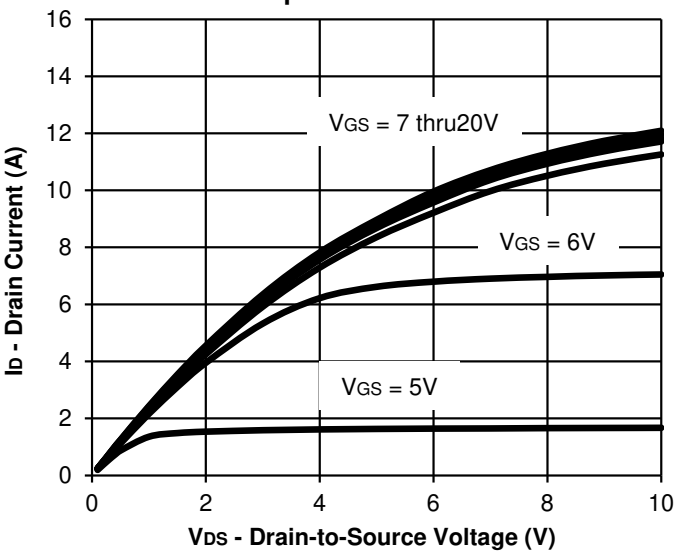
Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Thermal characteristics						
Thermal resistance, junction-case [a]	R_{thJC}		-	-	1.32	°C/W
Thermal resistance, junction-ambient [a]	R_{thJA}	leaded	-	-	62	
Soldering temperature, wave soldering only allowed at leads	T_{sold}	1.6mm (0.063in.) from case for 10 s	-	-	260	°C

Electrical characteristics at T_j=25°C, unless otherwise specified

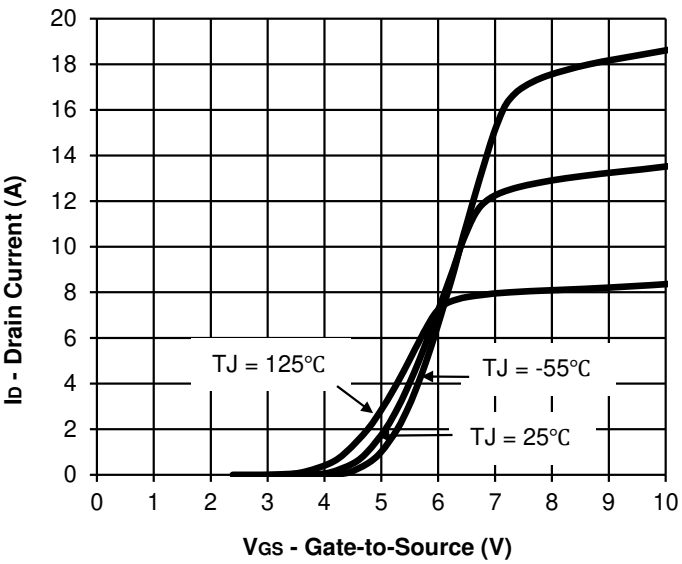
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=250μA	600	650	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	2.1	3.0	3.9	
Zero gate voltage drain current	I_{DSS}	V_{DS}=600V, V_{GS}=0V, T_j=25°C	-	0.1	1	μA
		V_{DS}=600V, V_{GS}=0V, T_j=150°C	-	100	-	
Gate source leakage current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0V	-	-	100	nA
Drain-source on-state resistance	$R_{DS\ (on)}$	V_{GS}=10V, I_D=4A, T_j=25°C	-	0.43	0.52	Ω
		V_{GS}=10V, I_D=4A, T_j=150°C	-	1.21	-	
Gate resistance	R_G	f=1 MHZ, open drain	-	4.1	-	Ω
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, f=1 MHz; V_{DS}=25 V	-	865	-	pF
Output capacitance	C_{oss}	V_{DS}=100 V	-	36	-	
Reverse transfer capacitance	C_{rss}	V_{DS}=25 V	-	4.7	-	
Transconductance	g_{fs}	V_{DS}>2*I_D*R_{DS}, I_D=4A	-	5.5	-	S
Turn-on delay time	$t_{d(on)}$	V_{DS}=380V, V_{GS}=10V, I_D=4A, R_G=4Ω (External)	-	10.6	-	ns
Rise time	t_r		-	13.2	-	
Turn-off delay time	$t_{d(off)}$		-	33.3	-	
Fall time	t_f		-	5.2	-	

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Gate charge characteristics						
Gate to source charge	Q_{gs}	V_{DS}=480 V, I_D=8A, V_{GS}=0 to 10 V	-	7.5	-	nC
Gate to drain charge	Q_{gd}		-	7.6	-	
Gate charge total	Q_g		-	23	-	
Gate plateau voltage	$V_{plateau}$		-	6.7	-	V
Reverse Diode						
Continuous forward current	I_S	V_{GS}=0V	-	-	8	A
Diode forward voltage	V_{SD}	V_{GS}=0V, $I_{S=}I_F$	-	0.9	1.2	V
Reverse recovery time	t_{rr}	V_{RR}=480V, $I_{S=}I_F$, d_{iF}/d_t=100 A/µS	-	193.5	-	ns
Reverse recovery charge	Q_{rr}		-	2.2	-	µC
Peak reverse recovery current	I_{rm}		-	27	-	A

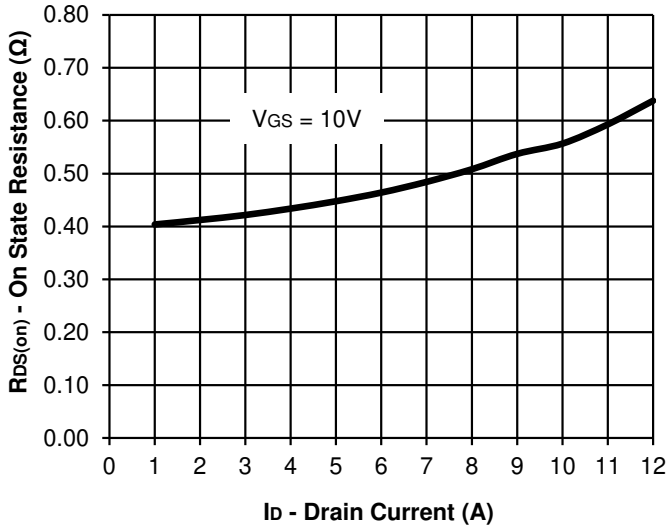
Output Characteristics



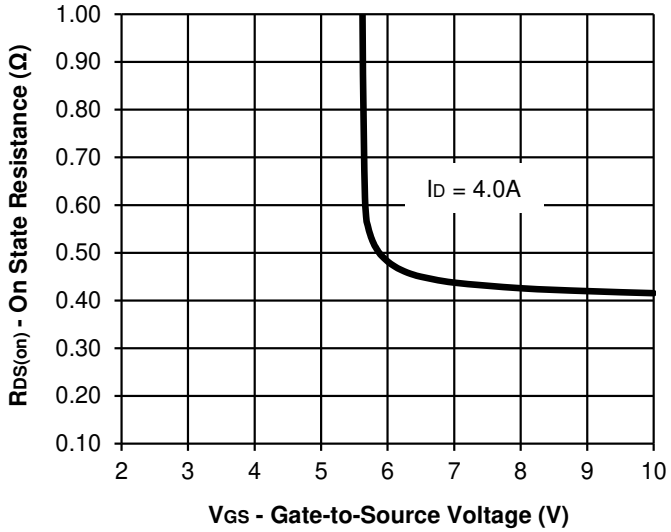
Transfer Characteristics



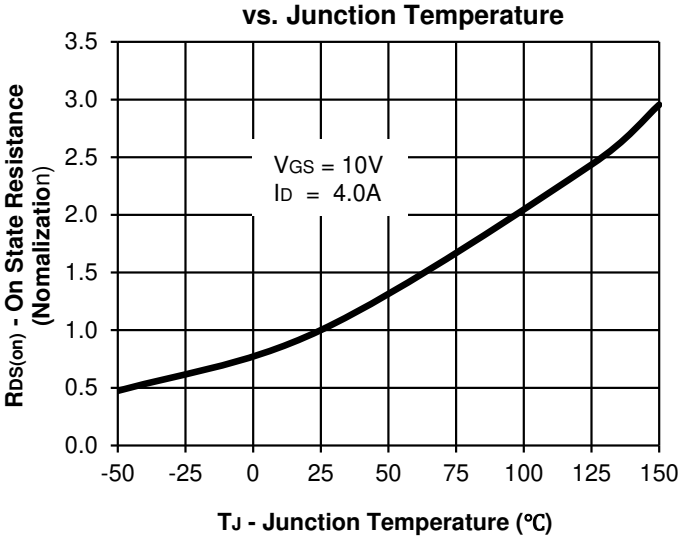
Drain - Source On-State Resistance vs. Drain Current



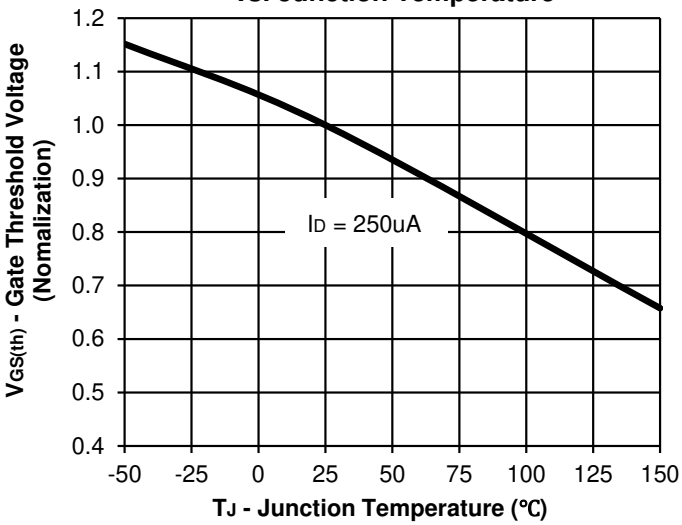
Drain-Source On-State Resistance vs. Gate-to-Source Voltage



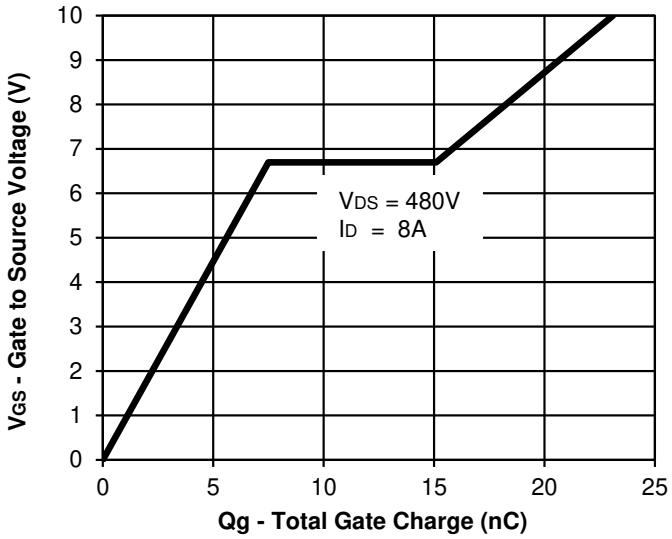
Drain - Source On State Resistance vs. Junction Temperature



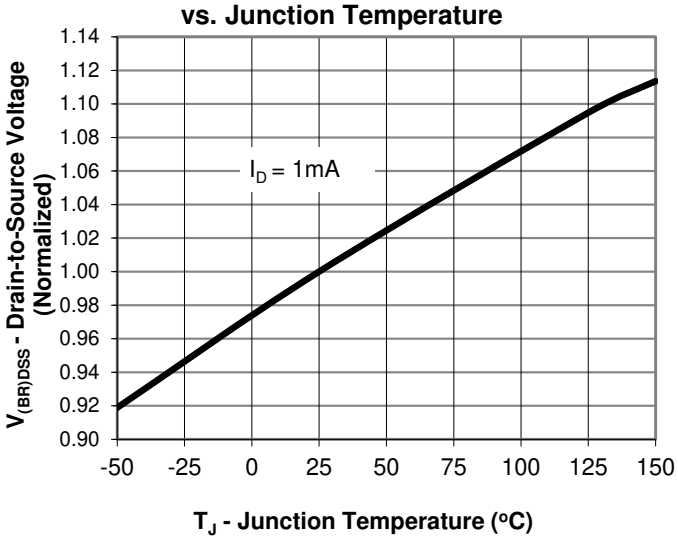
Gate Threshold Voltage vs. Junction Temperature



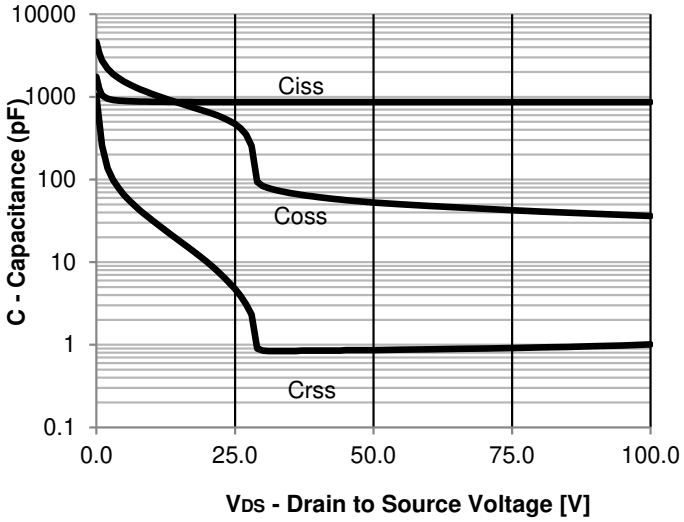
Gate Charge



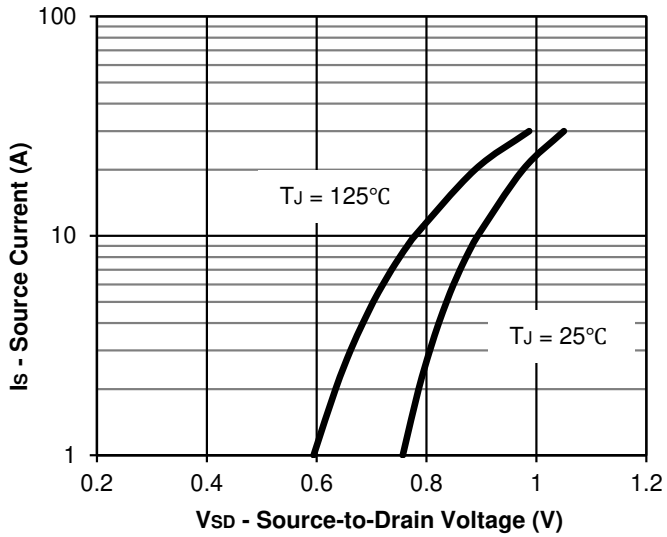
Drain-toSource Breakdown Voltage vs. Junction Temperature



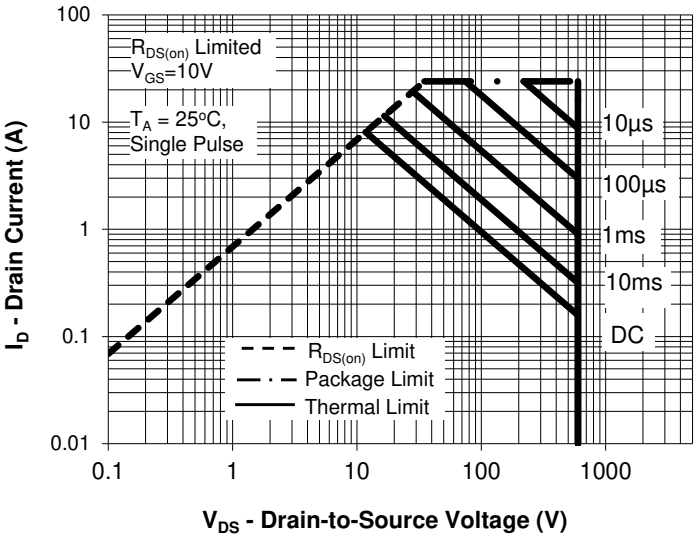
Capacitance



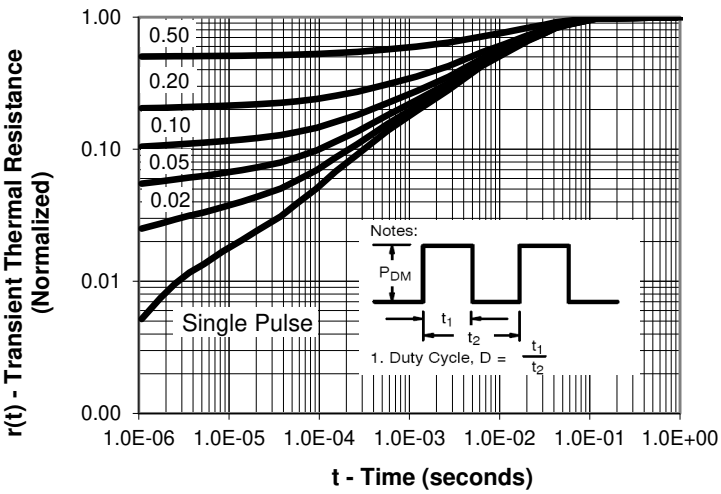
Source-Drain Diode Forward Voltage



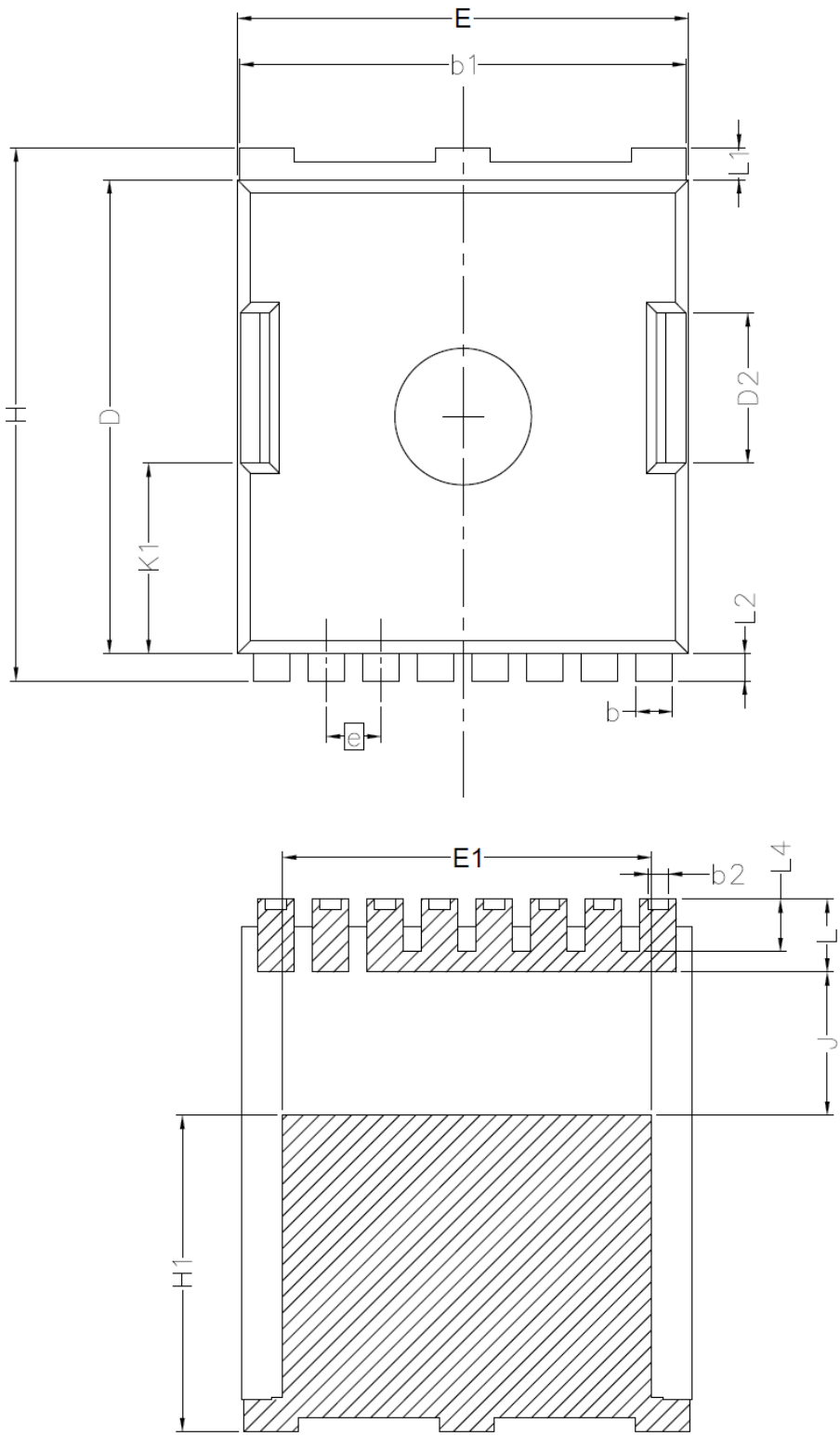
Maximum Rated Forward Biased Safe Operating Area



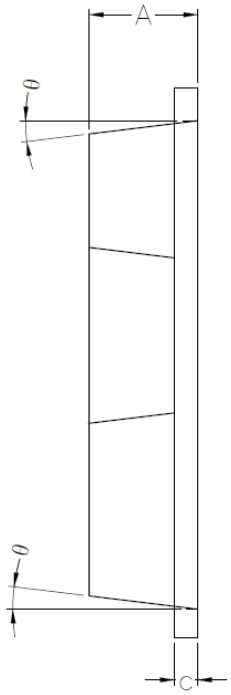
Transient Thermal Response, Junction-to-Case

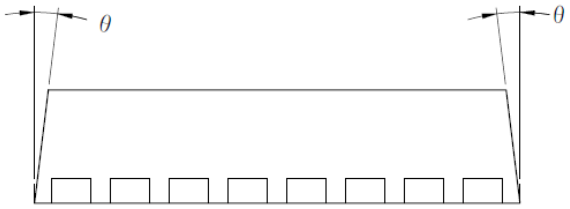


Package Outline: TOLL



Package Outline: TOLL





Symbol	Min	Nom	Max
A	2.2	2.3	2.4
b	0.7	0.8	0.9
b1	9.7	9.8	9.9
b2	0.42	0.46	0.5
c	0.4	0.5	0.6
D	10.28	10.43	10.58
D2	3.1	3.3	3.5
E	9.7	9.9	10.1
E1	7.9	8.1	8.3
e		1.20 BSC	
H	11.48	11.68	11.88
H1	6.75	6.95	7.15
N		8	
J	3	3.15	3.3
K1	3.98	4.18	4.38
L	1.4	1.6	1.8
L1	0.6	0.7	0.8
L2	0.5	0.6	0.7
L4	1	1.15	1.3
θ	4°	6°	10°

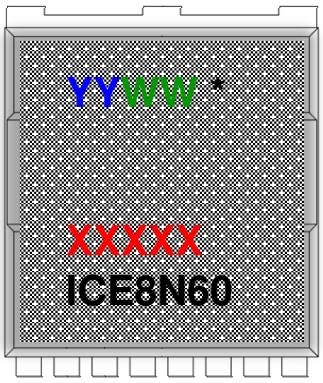
Marking Information

YY = Last two digits of the year

WW = Work week

* = Site ID

XXXXXX = Lot ID



ICE8N60 = ICE is IceMOS logo and
8N60 is a designated device part number

Disclaimer