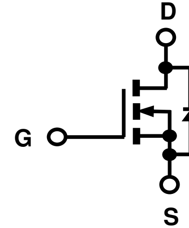
ICE8N60D

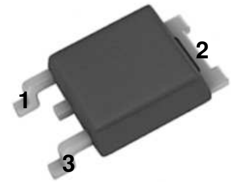
ICE8N60D N-Channel Enhancement Mode MOSFET

Product Summary			
I_D	T_A=25°C	8A	Max
$V_{(BR)DSS}$	I_D=250uA	600V	Min
$r_{DS(on)}$	V_{GS}=10V	0.43	Typ
Q_g	V_{DS}=480V	23nC	Typ

Features

- Low $r_{DS(on)}$
- Ultra Low Gate Charge
- High d*v*/d*t* capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems





T0252

Standard Metal Heatsink

1=Gate, 2=Drain, 3=Source.

ICEMOS OWNS THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 to 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN & EUROPE.

Maximum ratings [a] at T_j=25°C, unless otherwise specified

Parameter	*Symbol*	*Conditions*	*Value*	*Unit*
Continuous drain current	I_D	T_c=25°C	8	A
		T_c=100°C	5	
Pulsed drain current	$I_{D,\ pulse}$	T_c=25°C	24	A
Avalanche energy, single pulse	E_{AS}	I_D=5.6A	156	mJ
Avalanche current, repetitive	I_{AR}	limited by $T_j$max	5.6	A
MOSFET d*v*/d*t* ruggedness	d*v*/d*t*	V_{DS}=480V, I_D=8A, T_j=125°C	50	V/ns
Gate source voltage	V_{GS}	Static	±20	V
		AC (*f*>1Hz)	±30	
Power dissipation	P_{tot}	T_c=25°C	95	W
Operating and storage temperature	T_j, T_{stg}		-55 to +150	°C

a limited by T_{jmax}

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Thermal characteristics						
Thermal resistance, junction-case [a]	R_{thJC}		-	-	1.32	°C/W
Thermal resistance, junction-ambient [a]	R_{thJA}	leaded	-	-	62	°C/W
Soldering temperature, wave soldering only allowed at leads	T_{sold}	1.6mm (0.063in.) from case for 10 s	-	-	260	°C

Electrical characteristics at T_j=25°C, unless otherwise specified

Static characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=250µA	600	650	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250µA	2.1	3.0	3.9	V
Zero gate voltage drain current	I_{DSS}	V_{DS}=600V, V_{GS}=0V, T_j=25°C	-	0.1	1	µA
		V_{DS}=600V, V_{GS}=0V, T_j=150°C	-	100	-	
Gate source leakage current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0V	-	-	100	nA
Drain-source on-state resistance	$R_{DS\ (on)}$	V_{GS}=10V, I_D=4A, T_j=25°C	-	0.43	0.52	Ω
		V_{GS}=10V, I_D=4A, T_j=150°C	-	1.21	-	
Gate resistance	R_G	f=1 MHZ, open drain	-	4.1	-	Ω

Dynamic characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Input capacitance	C_{iss}	V_{GS}=0 V, f=1 MHz	V_{DS}=25 V	-	865	-	pF
Output capacitance	C_{oss}		V_{DS}=100 V	-	36	-	
Reverse transfer capacitance	C_{rss}		V_{DS}=25 V	-	4.7	-	
Transconductance	g_{fs}	V_{DS}>2*I_D*R_{DS}, I_D=4A		-	5.5	-	S
Turn-on delay time	$t_{d(on)}$	V_{DS}=380V, V_{GS}=10V, I_D=4A, R_G=4Ω (External)		-	10.6	-	ns
Rise time	t_r			-	13.2	-	
Turn-off delay time	$t_{d(off)}$			-	33.3	-	
Fall time	t_f			-	5.2	-	

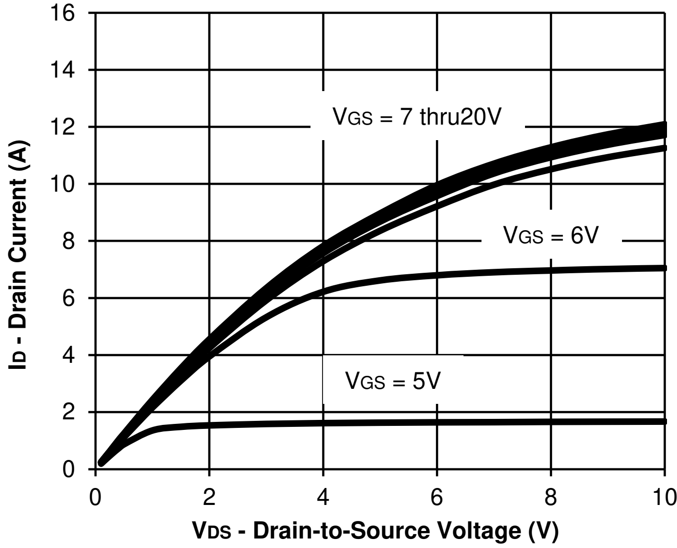
Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

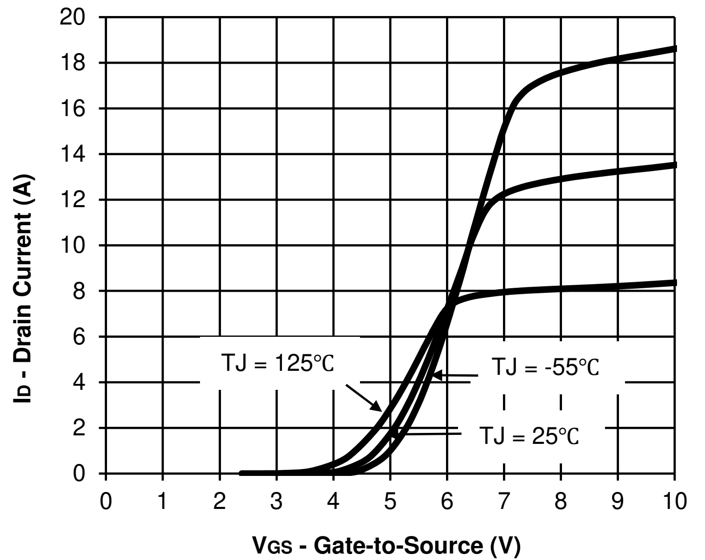
Gate charge characteristics

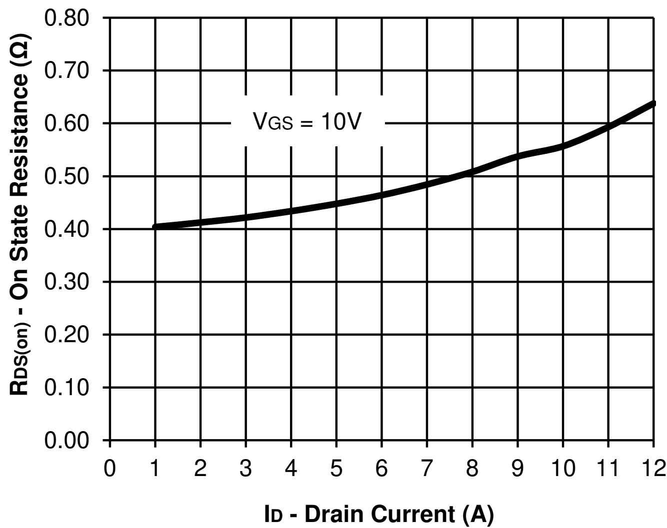
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Gate to source charge	Q_{gs}	V_{DS}=480 V, I_D=8A, V_{GS}=0 to 10 V	-	7.5	-	nC
Gate to drain charge	Q_{gd}		-	7.6	-	
Gate charge total	Q_g		-	23	-	
Gate plateau voltage	$V_{plateau}$		-	6.7	-	V

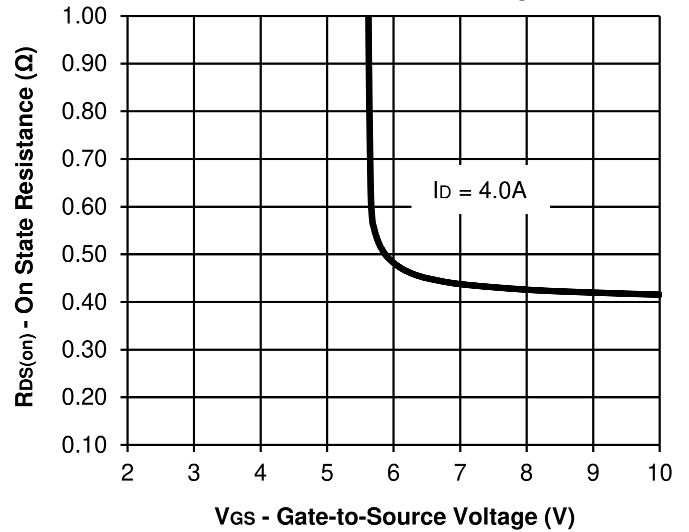
Reverse Diode

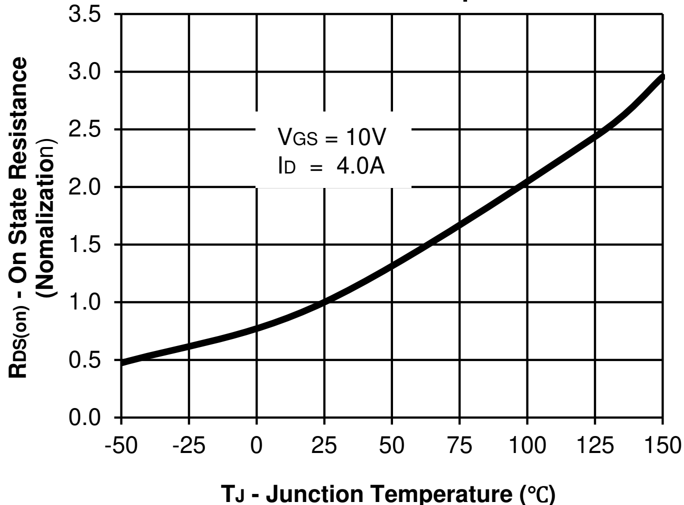
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Continuous forward current	I_S	V_{GS}=0V	-	-	8	A
Diode forward voltage	V_{SD}	V_{GS}=0V, $I_{S=}I_F$	-	0.9	1.2	V
Reverse recovery time	t_{rr}	V_{RR}=480V, $I_{S=}I_F$, d_{iF}/d_t=100 A/µS	-	193.5	-	ns
Reverse recovery charge	Q_{rr}		-	2.2	-	µC
Peak reverse recovery current	I_{rm}		-	27	-	A

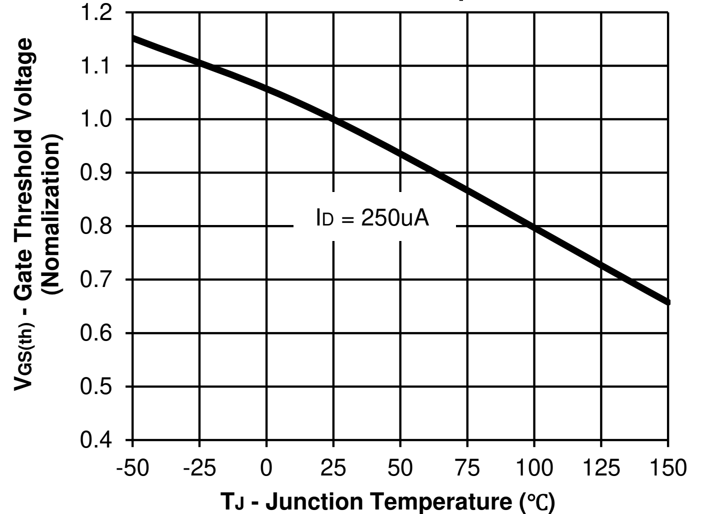

Output Characteristics
VGS = 7 thru20V
VGS = 6V
VGS = 5V
ID - Drain Current (A)
VDS - Drain-to-Source Voltage (V)

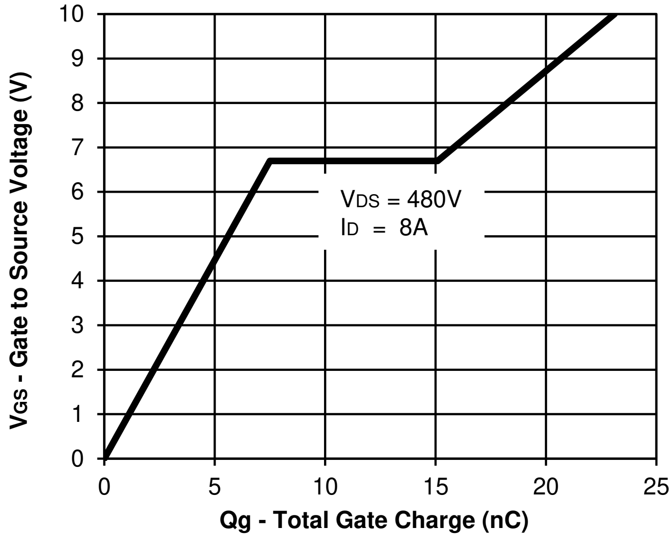

Transfer Characteristics
TJ = 125℃
TJ = -55℃
TJ = 25℃
ID - Drain Current (A)
VGS - Gate-to-Source (V)

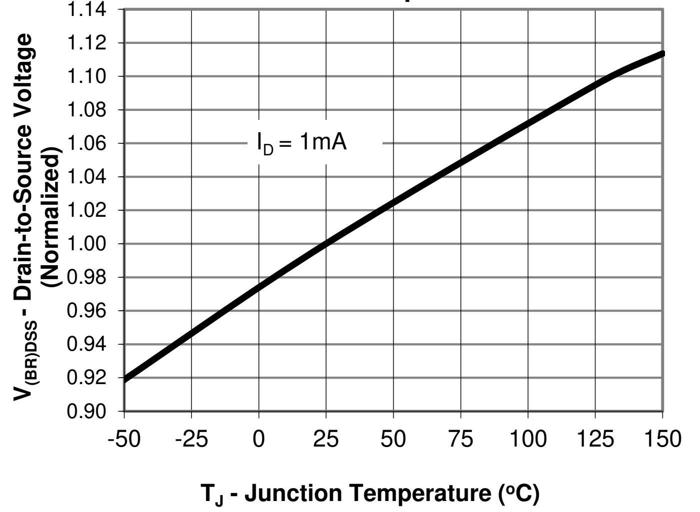

Drain - Source On-State Resistance
vs. Drain Current
VGS = 10V
RDS(on) - On State Resistance (Ω)
ID - Drain Current (A)

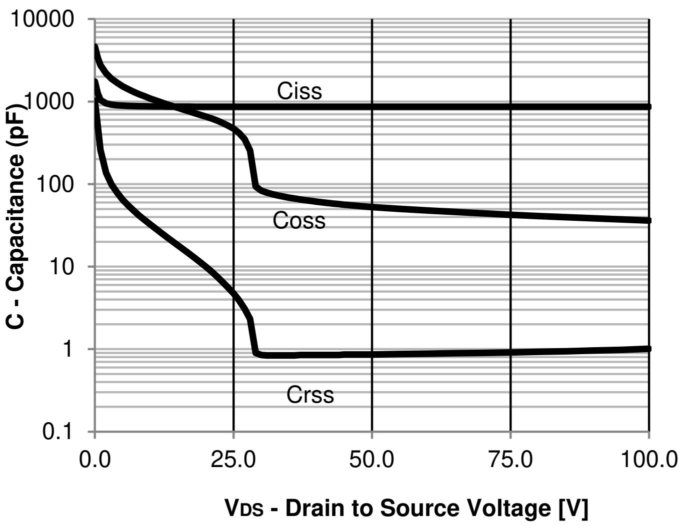

Drain-Source On-State Resistance
vs. Gate-to-Source Voltage
ID = 4.0A
RDS(on) - On State Resistance (Ω)
VGS - Gate-to-Source Voltage (V)

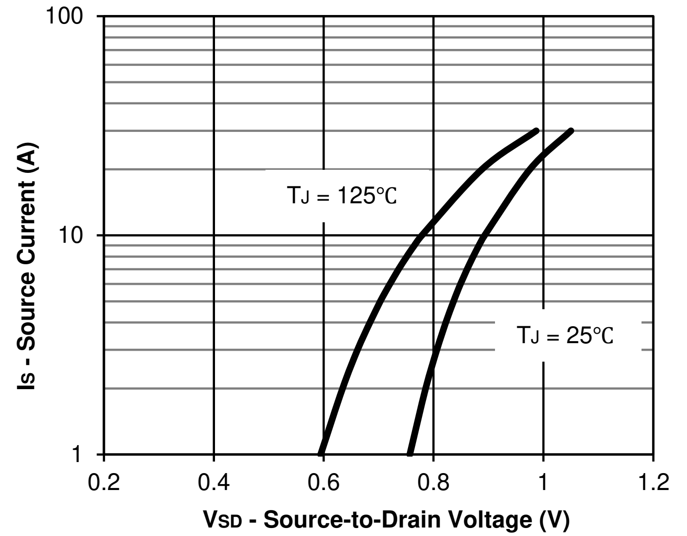

Drain - Source On State Resistance
vs. Junction Temperature
VGS = 10V
ID = 4.0A
RDS(on) - On State Resistance
(Nomalization)
TJ - Junction Temperature (℃)

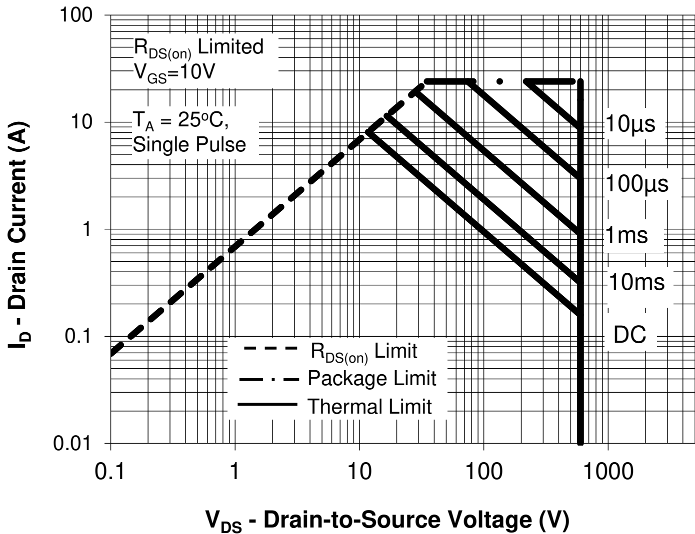

Gate Threshold Voltage
vs. Junction Temperature
ID = 250uA
VGS(th) - Gate Threshold Voltage
(Nomalization)
TJ - Junction Temperature (℃)

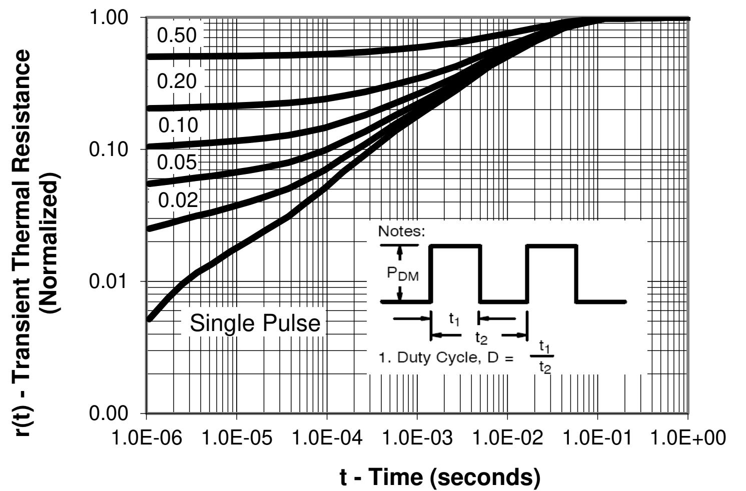

Gate Charge
VDS = 480V
ID = 8A
VGS - Gate to Source Voltage (V)
Qg - Total Gate Charge (nC)


Drain-toSource Breakdown Voltage vs. Junction Temperature
ID = 1mA
V(BR)DSS - Drain-to-Source Voltage (Normalized)
TJ - Junction Temperature (°C)

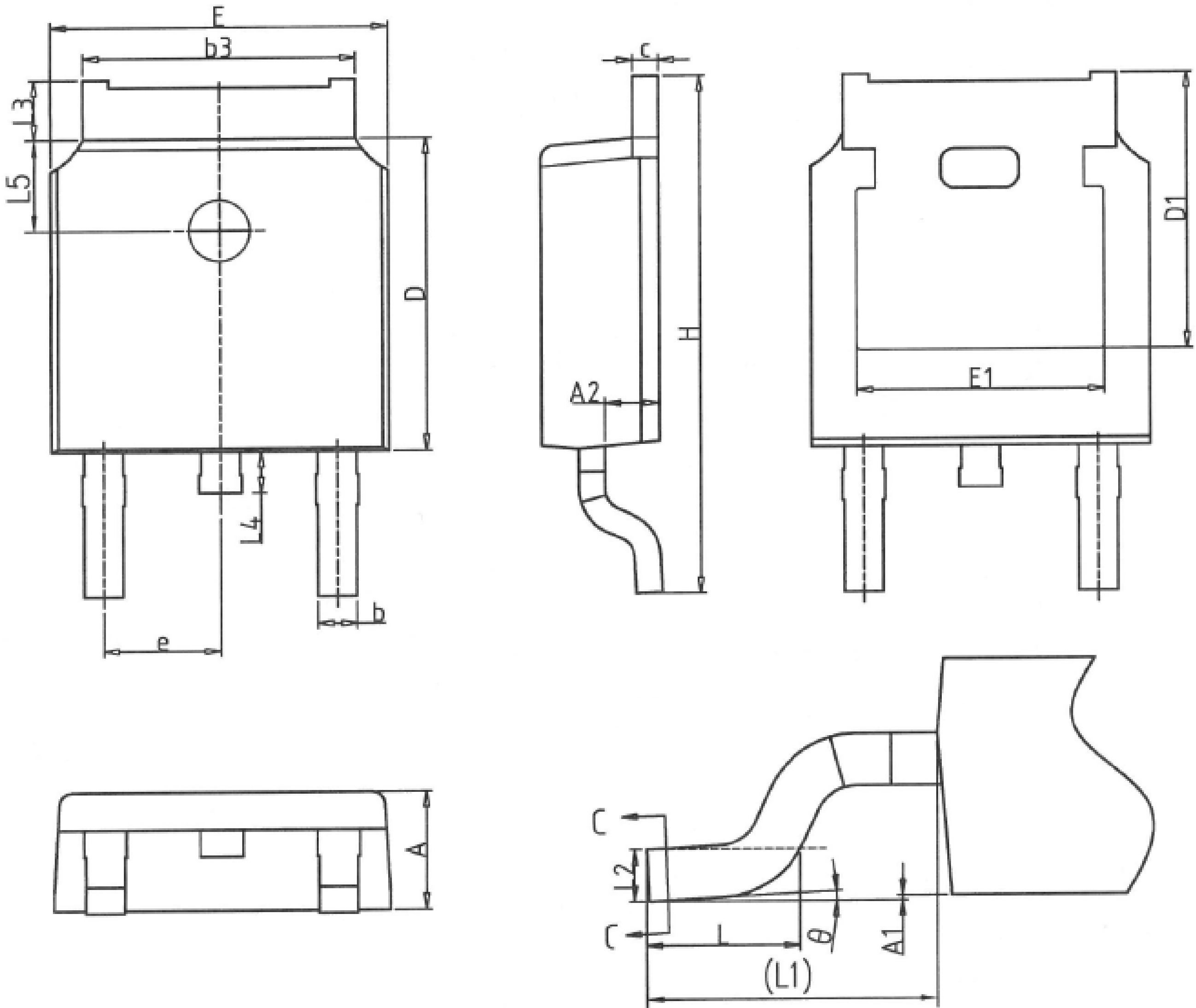

Capacitance
Ciss
Coss
Crss
C - Capacitance (pF)
VDS - Drain to Source Voltage [V]


Source-Drain Diode Forward Voltage
TJ = 125℃
TJ = 25℃
IS - Source Current (A)
VSD - Source-to-Drain Voltage (V)


Maximum Rated Forward Biased Safe Operating Area
RDS(on) Limited
VGS=10V
TA = 25°C,
Single Pulse
10µs
100µs
1ms
10ms
DC
RDS(on) Limit
Package Limit
Thermal Limit
ID - Drain Current (A)
VDS - Drain-to-Source Voltage (V)


Transient Thermal Response, Junction-to-Case
0.50
0.20
0.10
0.05
0.02
Single Pulse
Notes:
PDM
t1
t2
1. Duty Cycle, D = t1/t2
r(t) - Transient Thermal Resistance (Normalized)
t - Time (seconds)

Package Outline: TO252 (DPAK)



Package Outline: TO252 (DPAK)

SYMBOL	unit : mm		
	Min.	Nom.	Max
A	2.20	2.30	2.38
A1	0.00	-	0.20
A2	0.97	1.07	1.17
b	0.68	0.78	0.90
b3	5.20	5.33	5.46
c	0.43	0.53	0.61
D	5.98	6.10	6.22
D1	5.30REF		
E	6.40	6.60	6.73
E1	4.63	-	-
e	2.286BSC		
H	9.40	10.10	10.50
L	1.38	1.50	1.75
L1	2.90REF		
L2	0.51BSC		
L3	0.88	-	1.28
L4	0.50	-	1.00
L5	1.65	1.80	1.95
θ	0°		8°

Marking Information

YY = Last two digits of the year

WW = Work week

***** = Site ID

XXXXXX = Lot ID

ICE8N60 = ICE is IceMOS logo and
8N60 is a designated device part number

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