

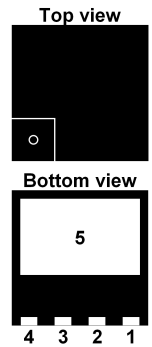
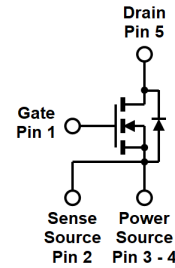
ICES14N60L N-Channel Enhancement Mode MOSFET

Features

- LOW $r_{DS(on)}$
- Ultra Low Gate Charge
- High dv/dt capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems



Product Summary			
I_D	$T_A=25^\circ\text{C}$	14A	Max
$V_{(BR)DSS}$	$I_D=250\mu\text{A}$	600V	Min
$r_{DS(on)}$	$V_{GS}=10\text{V}$	0.20	Typ
Q_g	$V_{DS}=480\text{V}$	52nC	Typ



DFN8x8

- 1 = Gate
2 = Sense Source
3 - 4 = Power Source
5 = Drain

ICEMOS OWNS THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 to 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN & EUROPE.

Maximum ratings^a, at $T_j=25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_c=25^\circ\text{C}$	14	A
		$T_c=100^\circ\text{C}$	9	
Pulsed drain current	$I_{D, \text{pulse}}$	$T_c=25^\circ\text{C}$	45	A
Avalanche energy, single pulse	E_{AS}	$I_D=9\text{A}$	400	mJ
Avalanche current, repetitive	I_{AR}	limited by $T_{j,max}$	9	A
MOSFET dv/dt ruggedness	dv/dt	$V_{DS}=480\text{V}$, $I_D=15\text{A}$, $T_j=125^\circ\text{C}$	50	V/ns
Gate source voltage	V_{GS}	Static	± 20	V
		AC ($f>1\text{Hz}$)	± 30	
Power dissipation	P_{tot}	$T_c=25^\circ\text{C}$	145	W
Operating and storage temperature	T_j, T_{stg}		-55 to +150	$^\circ\text{C}$

^a limited by $T_{j,max}$

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

Thermal characteristics

Thermal resistance, junction-case ^a	R_{thJC}		-	-	0.86	°C/W
Thermal resistance, junction-ambient ^a	R_{thJA}	lead	-	-	62	
Soldering temperature, wave soldering only allowed at leads	T_{solder}	1.6mm (0.063in.) from case for 10 s	-	-	260	°C

Electrical characteristics

, at $T_j=25^{\circ}\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=250\mu\text{A}$	600	640	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.1	3	3.9	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=600\text{V}, V_{GS}=0\text{V}, T_j=25^{\circ}\text{C}$	-	0.1	1	μA
		$V_{DS}=600\text{V}, V_{GS}=0\text{V}, T_j=150^{\circ}\text{C}$	-	100	-	
Gate source leakage current	I_{GSS}	$V_{GS}=\pm 20\text{ V}, V_{DS}=0\text{V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=7\text{A}, T_j=25^{\circ}\text{C}$	-	0.21	0.25	Ω
		$V_{GS}=10\text{V}, I_D=7\text{A}, T_j=150^{\circ}\text{C}$	-	0.56	-	
Gate resistance	R_G	$f=1\text{ MHz}, \text{open drain}$	-	3	-	Ω

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V},$ $f=1\text{ MHz}$	$V_{DS}=25\text{ V}$	-	1742	-	pF
Output capacitance	C_{oss}		$V_{DS}=100\text{ V}$	-	71	-	
Reverse transfer capacitance	C_{rss}		$V_{DS}=25\text{ V}$	-	12	-	
Transconductance	g_{fs}	$V_{DS}>2*I_D*R_{DS}, I_D=7A$		-	11	-	S
Turn-on delay time	$t_{d(on)}$	$V_{DS}=380V, V_{GS}=10V,$ $I_D=7A, R_G=4\Omega$ (External)		-	21	-	ns
Rise time	t_r			-	10	-	
Turn-off delay time	$t_{d(off)}$			-	88	-	
Fall time	t_f			-	5.2	-	

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

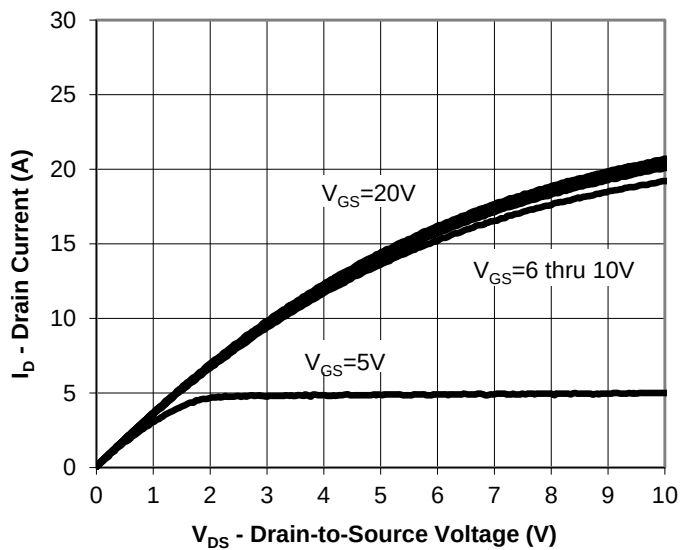
Gate charge characteristics

Gate to source charge	Q_{gs}	$V_{DS}=480\text{ V}, I_D=14\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	9	-	nC
Gate to drain charge	Q_{gd}		-	18	-	
Gate charge total	Q_g		-	52	-	
Gate plateau voltage	V_{plateau}		-	5.4	-	V

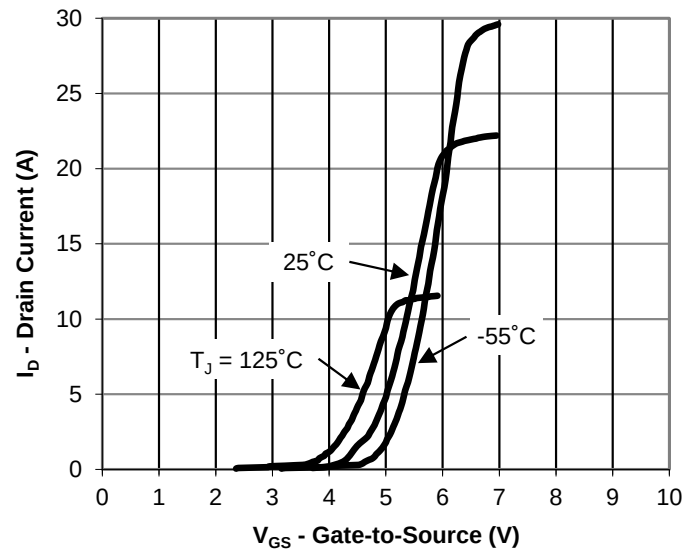
Reverse Diode

Continuous forward current	I_S	$V_{GS}=0\text{ V}$	-	-	14	A
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_S=I_F$	-	0.9	1.2	V
Reverse recovery time	t_{rr}	$V_{RR}=300\text{ V}, I_S=I_F,$ $d_{iF}/d_t=100\text{ A}/\mu\text{S}$	-	340	-	ns
Reverse recovery charge	Q_{rr}		-	5.6	-	μC
Peak reverse recovery current	I_{rm}		-	29	-	A

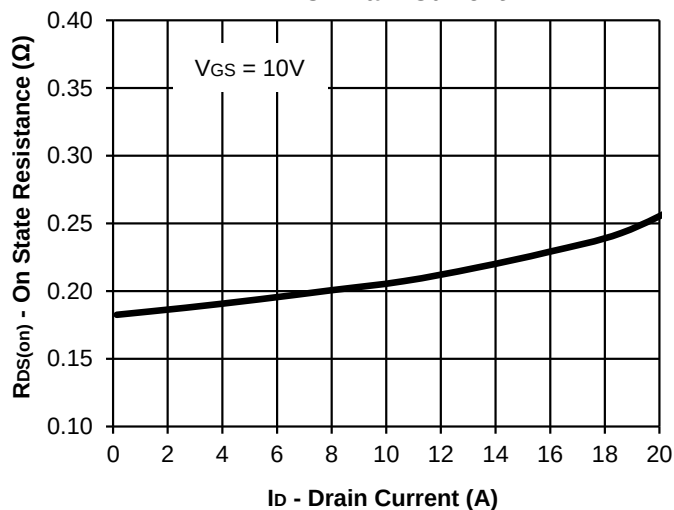
Output Characteristics



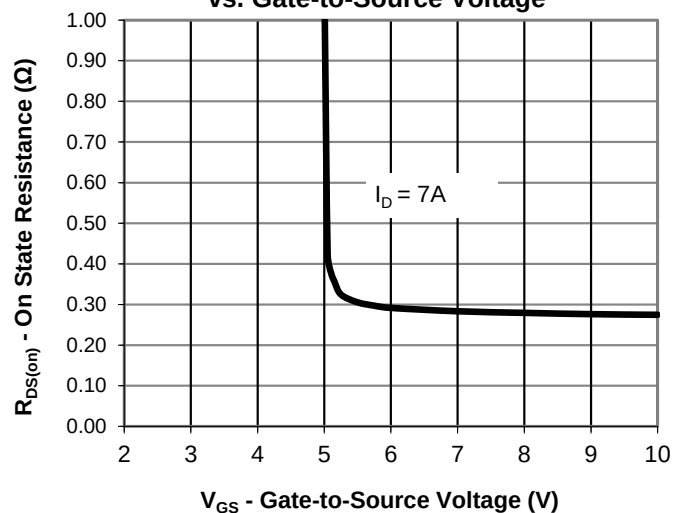
Transfer Characteristics



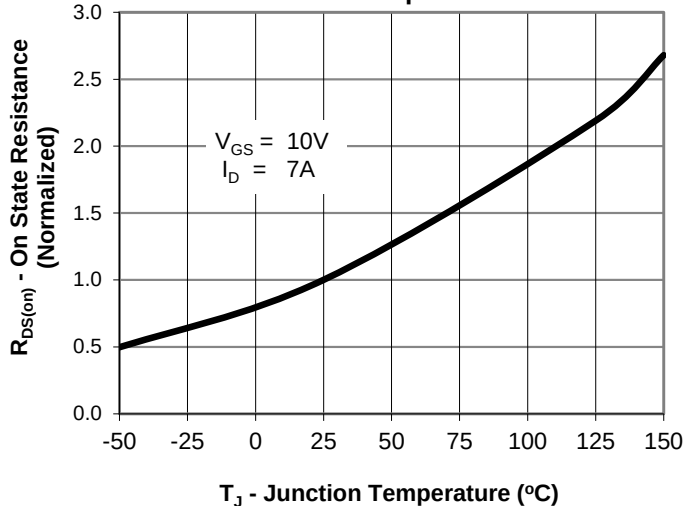
Drain - Source On-State Resistance vs. Drain Current



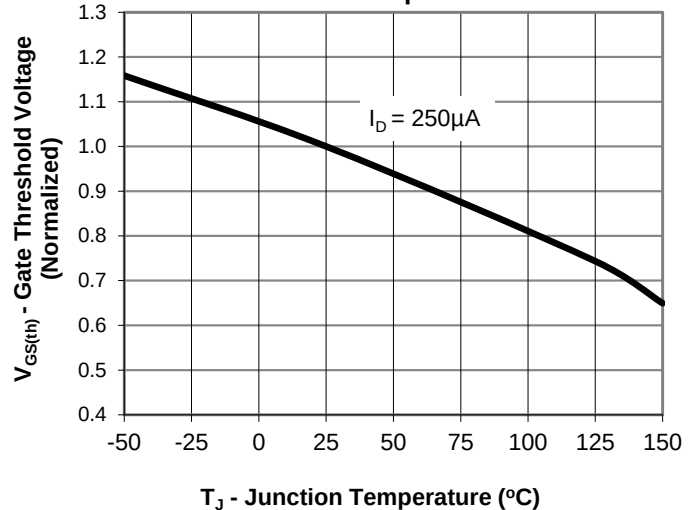
Drain-Source On-State Resistance vs. Gate-to-Source Voltage



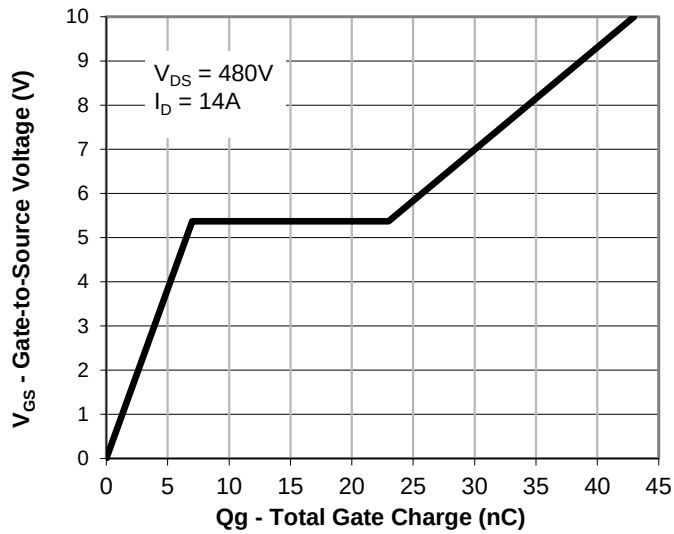
Drain-Source On State Resistance vs. Junction Temperature



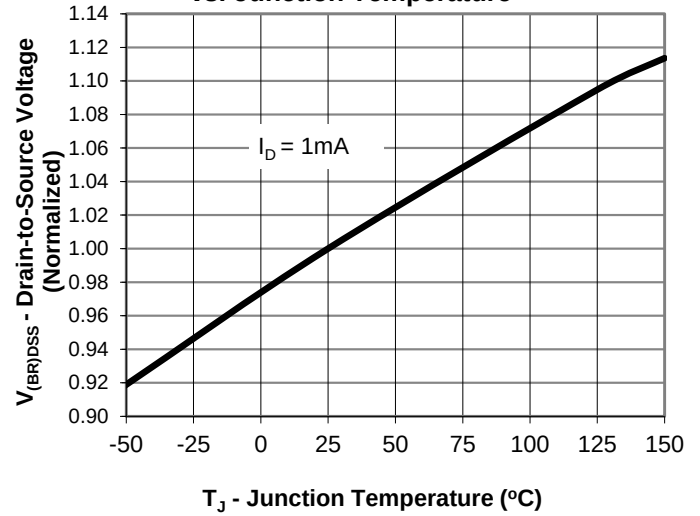
Gate Threshold Voltage vs. Junction Temperature



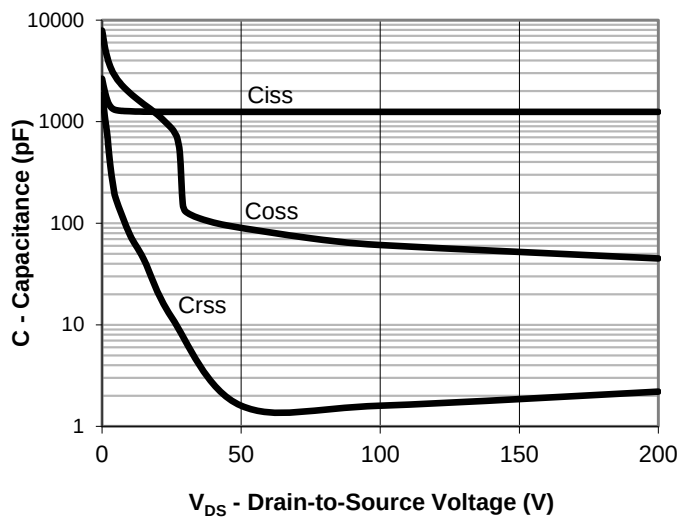
Gate Charge



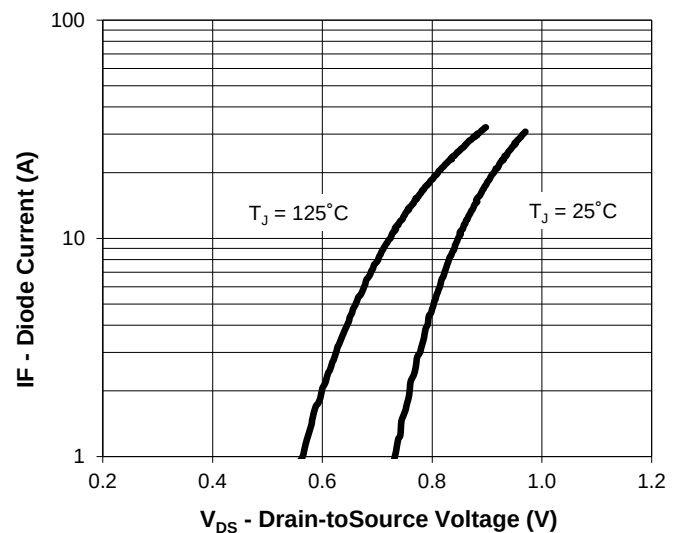
Drain-toSource Breakdown Voltage vs. Junction Temperature



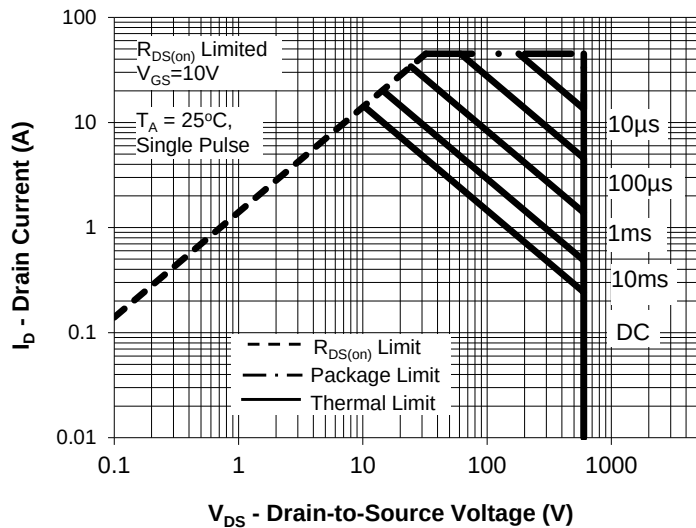
Capacitance



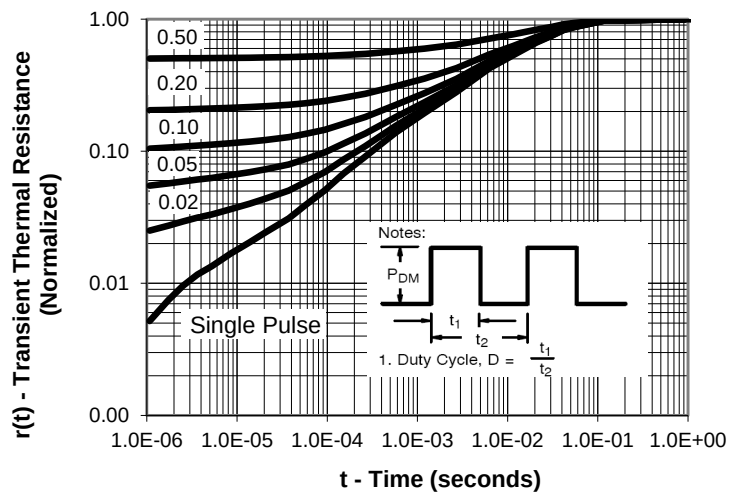
Drain-Source Diode Forward Voltage



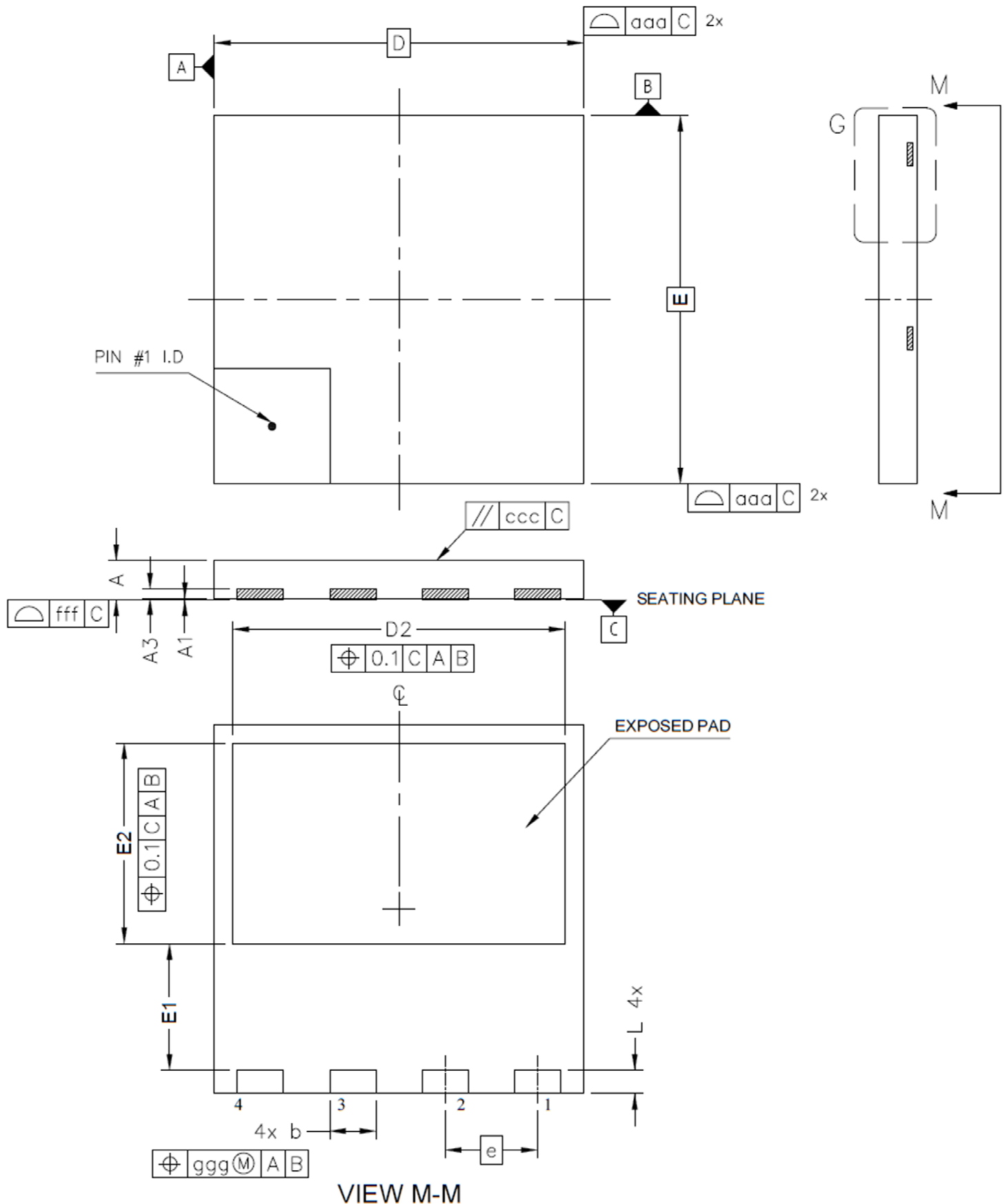
Maximum Rated Forward Biased Safe Operating Area



Transient Thermal Response, Junction-to-Case



Package Outline: DFN8x8

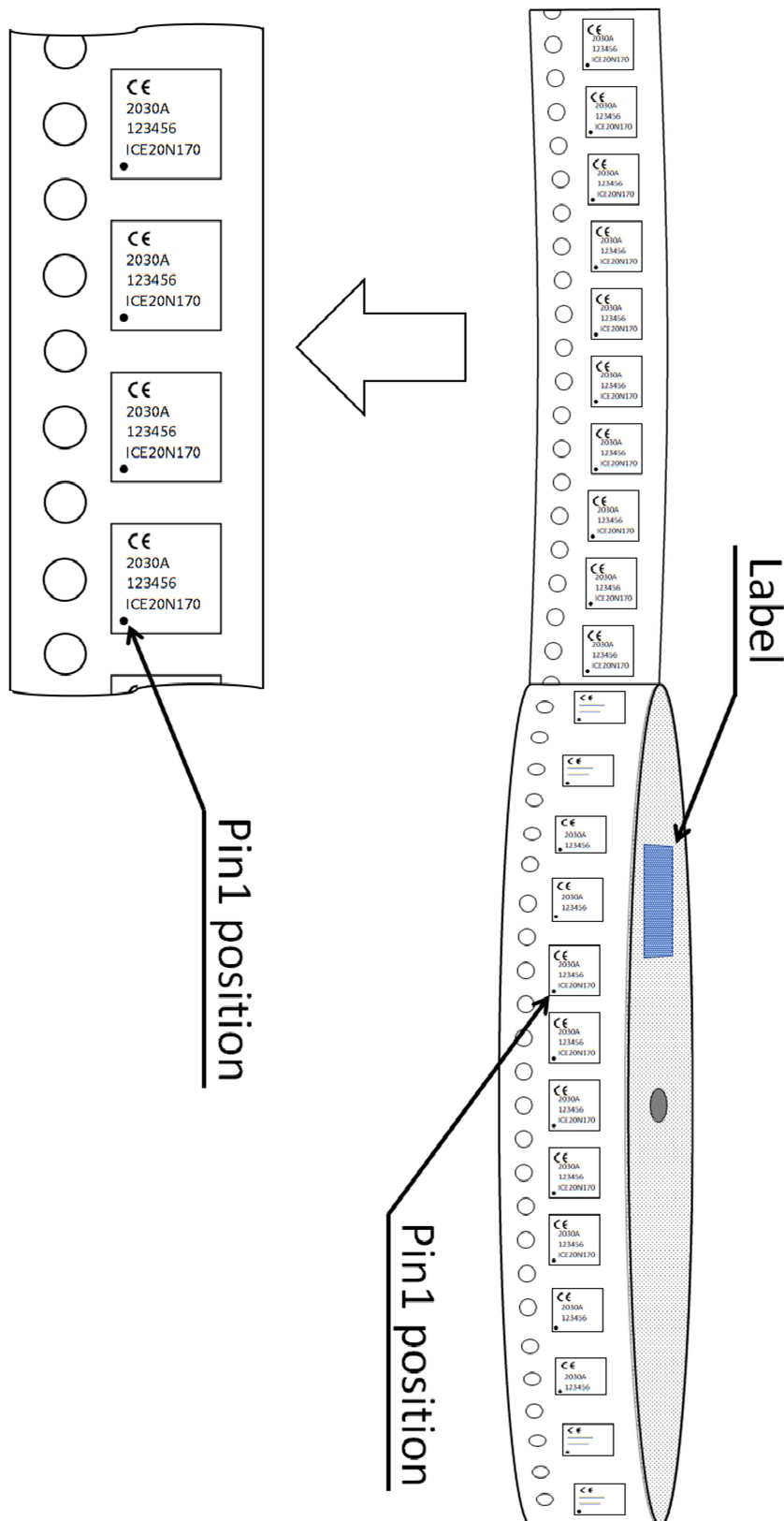


Package Outline: DFN8x8

SYMBOL	MIN	MAX	NOTES
A	0.75	0.95	1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
A1	0.00	0.05	
A3	0.10	0.30	2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
b	0.90	1.10	
D	7.90	8.10	3.0 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.90mm AND 1.10mm FROM TERMINAL TIP.
E	7.90	8.10	
D2	7.10	7.30	4.0 DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
E1	2.65	2.85	
E2	4.25	4.45	5.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
e	2.00 BSC		
L	0.40	0.60	6.0 RADIUS ON TERMINAL IS OPTIONAL.
aaa	0.10		
ggg	0.05		
ccc	0.05		
fff	0.05		

Tape and Reel : DFN8x8

Reel size : 13 inch
QTY per reel : 3000pcs



Marking Information

YY = Last two digits of the year

WW = Work week

***** = Site ID

XXXXXX = Lot ID



ICES14N60 = ICE is IceMOS logo and
S14N60 is a designated device part
number

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