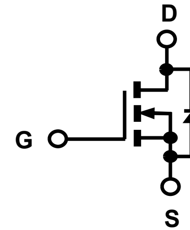
ICE8S65

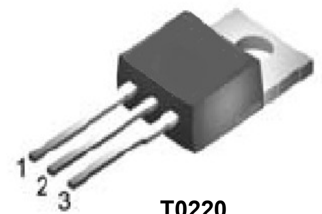
ICE8S65 N-Channel Enhancement Mode MOSFET

Product Summary			
I_D	T_A=25°C	8A	Max
BV_{DSS}	I_D=250uA	650V	Min
$r_{DS(on)}$	V_{GS}=10V	0.33Ω	Typ
Q_g	V_{DS}=480V	12.7nC	Typ

Features

- Low $r_{DS(on)}$
- Ultra Low Gate Charge
- High dv/dt capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Optimized design for hard switching SMPS topologies





T0220

Standard Metal Heatsink

1=Gate, 2=Drain, 3=Source.

Lead Free

ICEMOS AND ITS SISTER COMPANY 3D SEMI OWN THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 to 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN & EUROPE.

Maximum ratings [b] at T_j=25°C, unless otherwise specified

Parameter	*Symbol*	*Conditions*	*Value*	*Unit*
Continuous drain current	I_D	T_c=25°C T_c=100°C	8 5.0	A
Pulsed drain current	$I_{D,\ pulse}$	T_c=25°C	18	A
Avalanche energy, single pulse	E_{AS}	I_D=2.7A	40	mJ
Avalanche current, repetitive	I_{AR}	limited by $T_j$max	2.7	A
MOSFET dv/dt ruggedness	dv/dt	V_{DS}=480V, I_D=8A, T_j=125°C	50.0	V/ns
Gate source voltage	V_{GS}	Static	±20	V
		AC (f>1Hz)	±30	
Power dissipation	P_{tot}	T_c=25°C	78	W
Operating and storage temperature	T_j, T_{stg}		-55 to +150	°C
Mounting torque		M 3 screws	50	Ncm

a When mounted on 1inch square 2oz copper clad FR-4
b limited by T_{jmax}

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

Thermal characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Thermal resistance, junction-case [a]	R_{thJC}		-	-	1.6	°C/W
Thermal resistance, junction-ambient [a]	R_{thJA}	leaded	-	-	62	
Soldering temperature, wave soldering only allowed at leads	T_{sold}	1.6mm (0.063in.) from case for 10 s	-	-	260	°C

Electrical characteristics at T_j=25°C, unless otherwise specified

Static characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=250μA	650	700	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	2.1	3	3.9	
Zero gate voltage drain current	I_{DSS}	V_{DS}=650V, V_{GS}=0V, T_j=25°C	-	0.1	1	μA
		V_{DS}=650V, V_{GS}=0V, T_j=150°C	-	100	-	
Gate source leakage current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0V	-	-	100	nA
Drain-source on-state resistance	$r_{DS(on)}$	V_{GS}=10V, I_D=4A, T_j=25°C	-	0.33	0.40	Ω
		V_{GS}=10V, I_D=4A, T_j=150°C	-	0.90	-	
Gate resistance	R_G	f=1 MHZ, open drain	-	1.2	-	Ω

Dynamic characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Input capacitance	C_{iss}	V_{GS}=0 V, f=1 MHz	V_{DS}=25 V	-	674	-	pF
	C_{oss}		V_{DS}=100 V	-	30	-	
	C_{rss}		V_{DS}=25 V	-	1.54	-	
Transconductance	g_{fs}	V_{DS}>2*I_D*R_{DS}, I_D=4A		-	7.1	-	S
Turn-on delay time	$t_{d(on)}$	V_{DS}=380V, V_{GS}=10V, I_D=8A, R_G=4Ω (External)		-	8.6	-	ns
Rise time	t_r			-	6.1	-	
Turn-off delay time	$t_{d(off)}$			-	22.5	-	
Fall time	t_f			-	2.7	-	

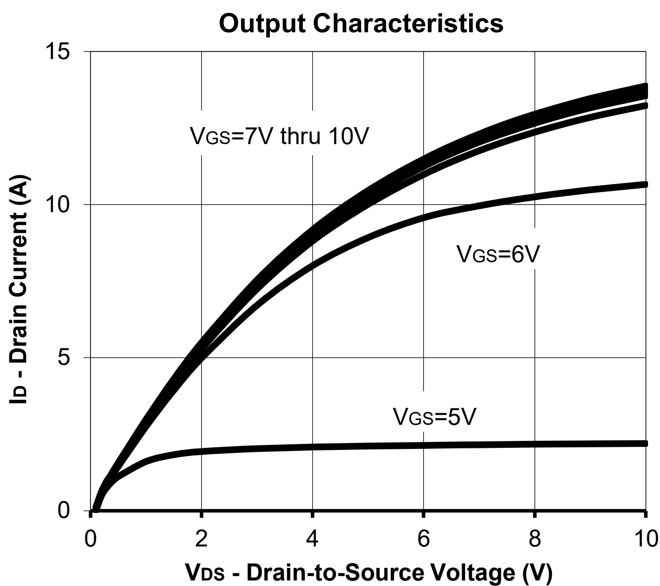
Parameter	*Symbol*	*Conditions*	*Values*			*Unit*
			Min	*Typ*	*Max*	

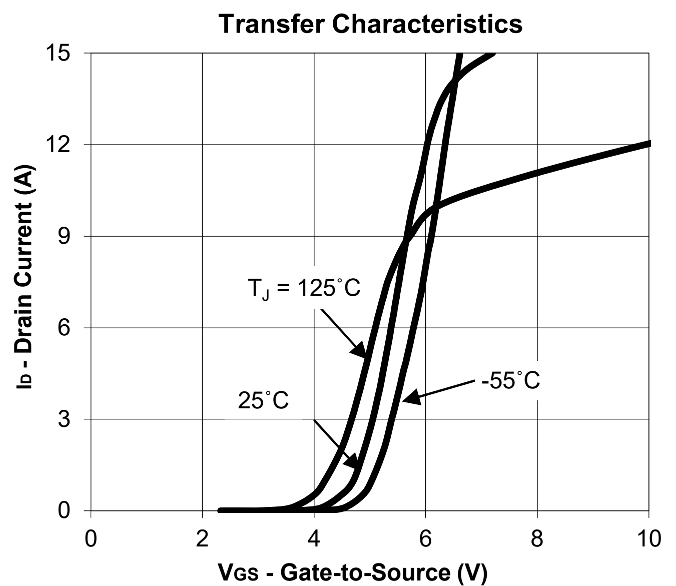
Gate charge characteristics

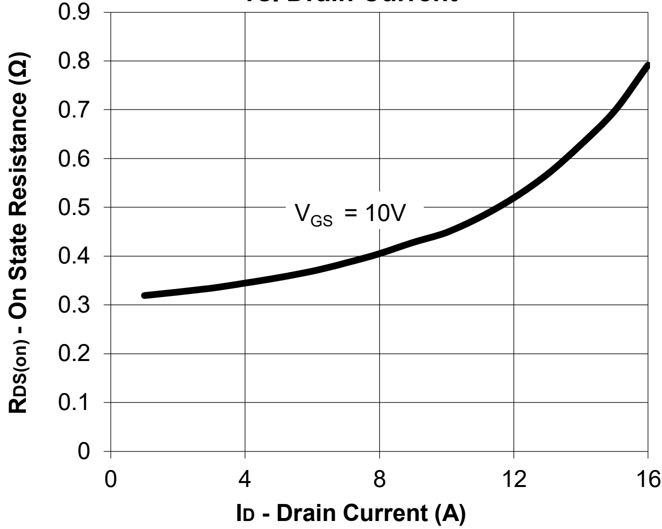
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Gate to source charge	Q_{gs}	V_{DS}=480 V, I_D=8A, V_{GS}=10 V	-	3.8	-	nC
Gate to drain charge	Q_{gd}		-	3.6	-	
Gate charge total	Q_g		-	12.7	-	
Gate plateau voltage	$V_{plateau}$		-	5.7	-	V

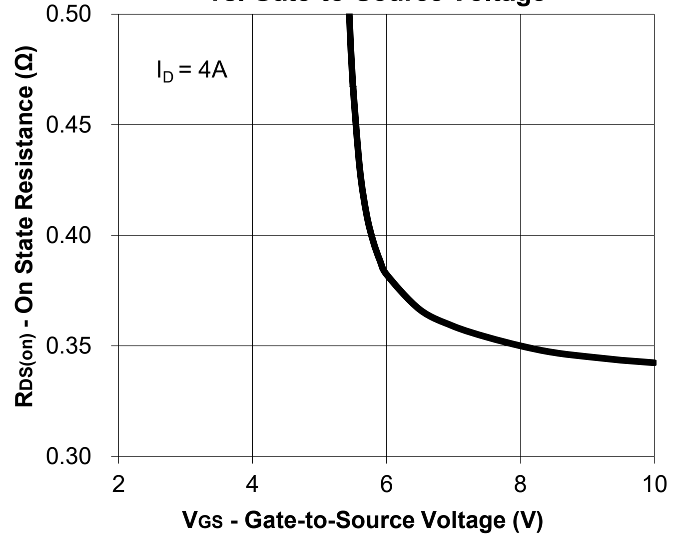
Reverse Diode

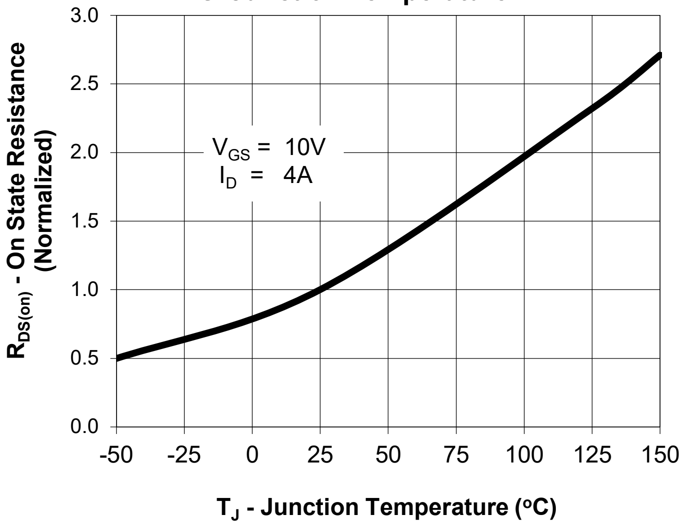
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Continuous forward current	I_S	V_{GS}=0V	-	-	8	A
Diode forward voltage	V_{SD}	V_{GS}=0V, I_S=I_F	-	0.9	1.2	V
Reverse recovery time	t_{rr}	V_{RR}=50V, I_S=I_F, d_{iF}/d_t=100 A/μS	-	308	-	ns
Reverse recovery charge	Q_{rr}		-	2	-	μC
Peak reverse recovery current	I_{rm}		-	13	-	A

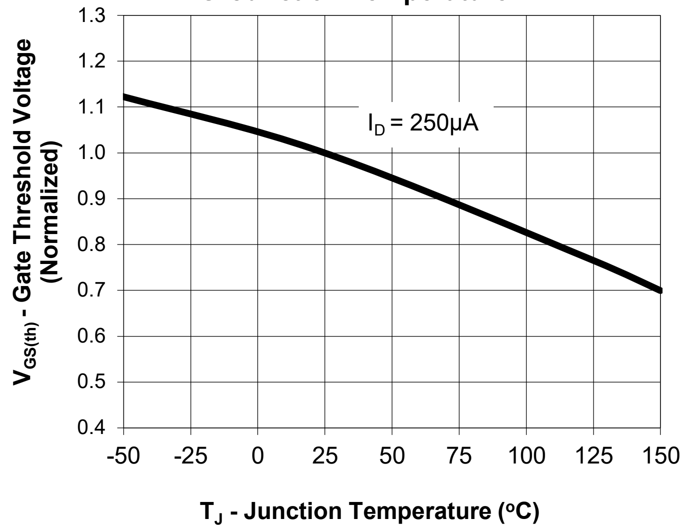


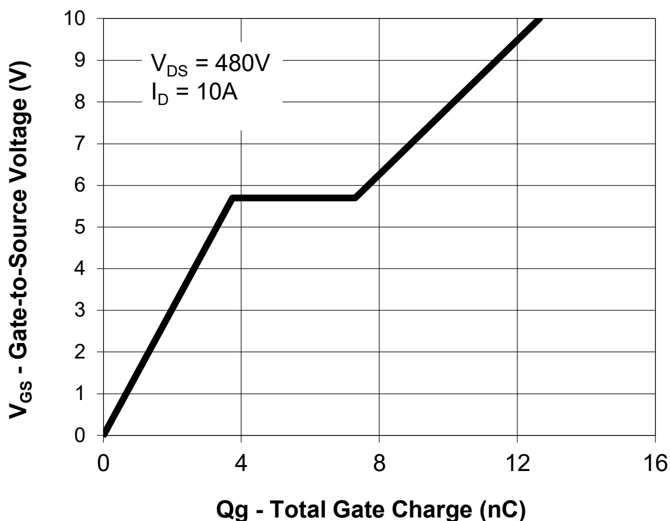


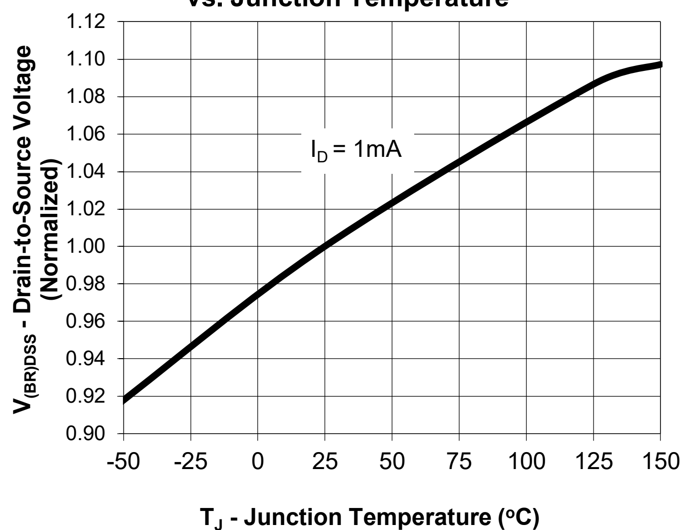

Drain - Source On-State Resistance
vs. Drain Current
RDS(on) - On State Resistance (Ω)
ID - Drain Current (A)
VGS = 10V
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
4
8
12
16

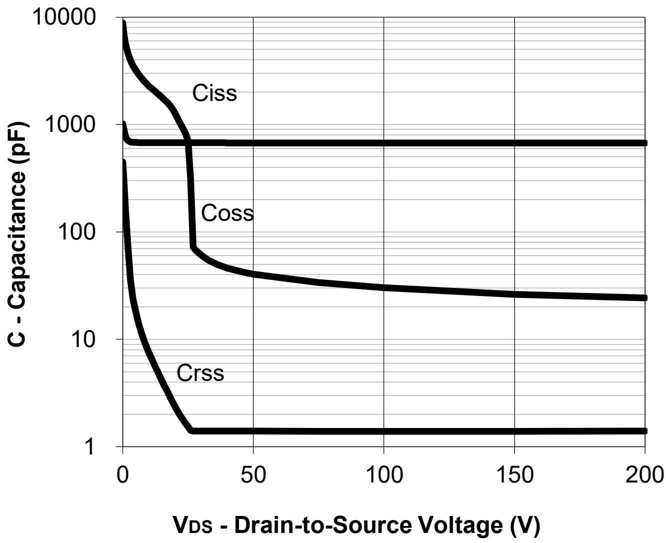

Drain-Source On-State Resistance
vs. Gate-to-Source Voltage
RDS(on) - On State Resistance (Ω)
VGS - Gate-to-Source Voltage (V)
ID = 4A
0.50
0.45
0.40
0.35
0.30
2
4
6
8
10

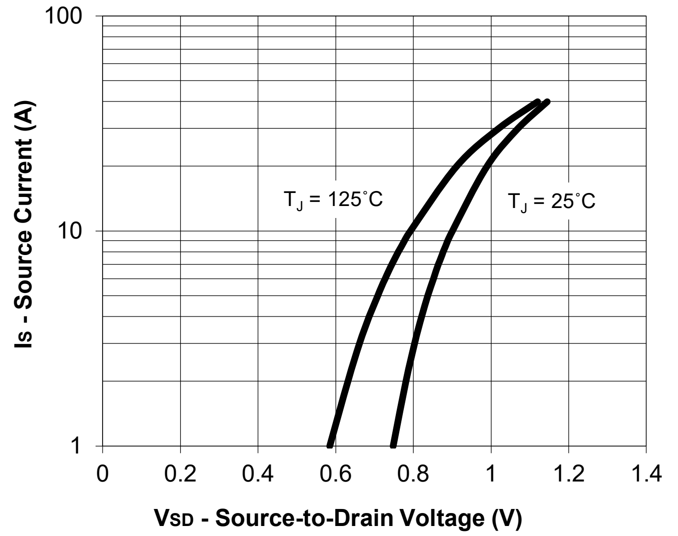

Drian-Source On State Resistance
vs. Junction Temperature
RDS(on) - On State Resistance
(Normalized)
TJ - Junction Temperature (°C)
VGS = 10V
ID = 4A
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-50
-25
0
25
50
75
100
125
150

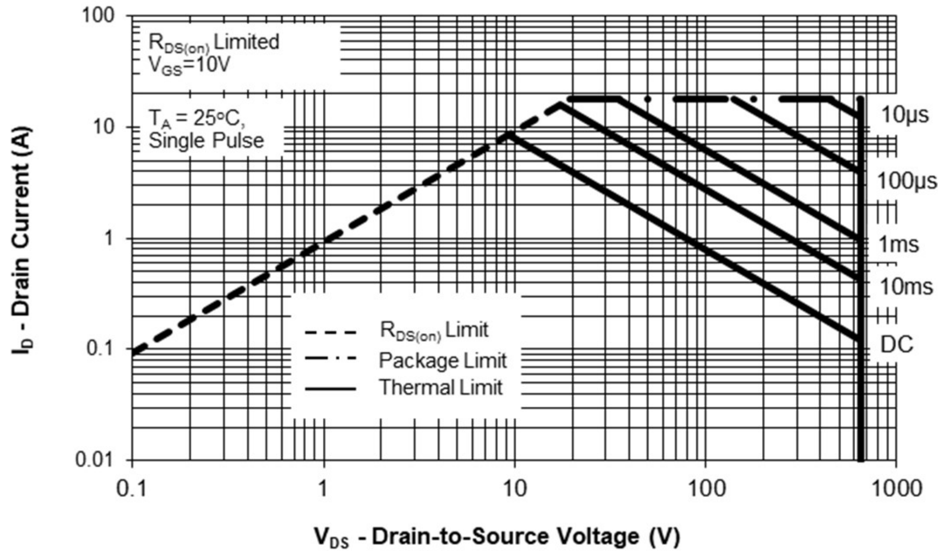

Gate Threshold Voltage
vs. Junction Temperature
VGS(th) - Gate Threshold Voltage
(Normalized)
TJ - Junction Temperature (°C)
ID = 250μA
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
-50
-25
0
25
50
75
100
125
150

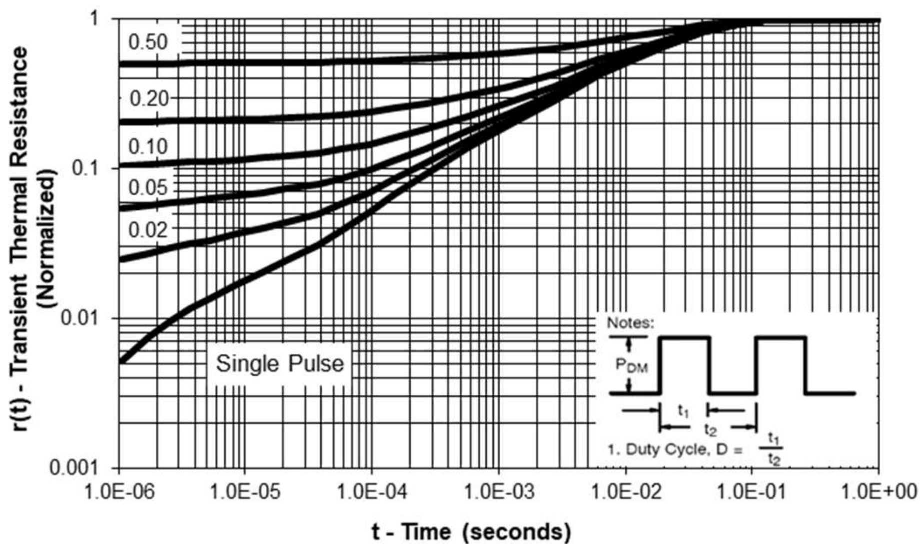

Gate Charge
VGS - Gate-to-Source Voltage (V)
Qg - Total Gate Charge (nC)
VDS = 480V
ID = 10A
10
9
8
7
6
5
4
3
2
1
0
0
4
8
12
16


Drain-toSource Breakdown Voltage
vs. Junction Temperature
V(BR)DSS - Drain-to-Source Voltage
(Normalized)
TJ - Junction Temperature (°C)
ID = 1mA
1.12
1.10
1.08
1.06
1.04
1.02
1.00
0.98
0.96
0.94
0.92
0.90
-50
-25
0
25
50
75
100
125
150

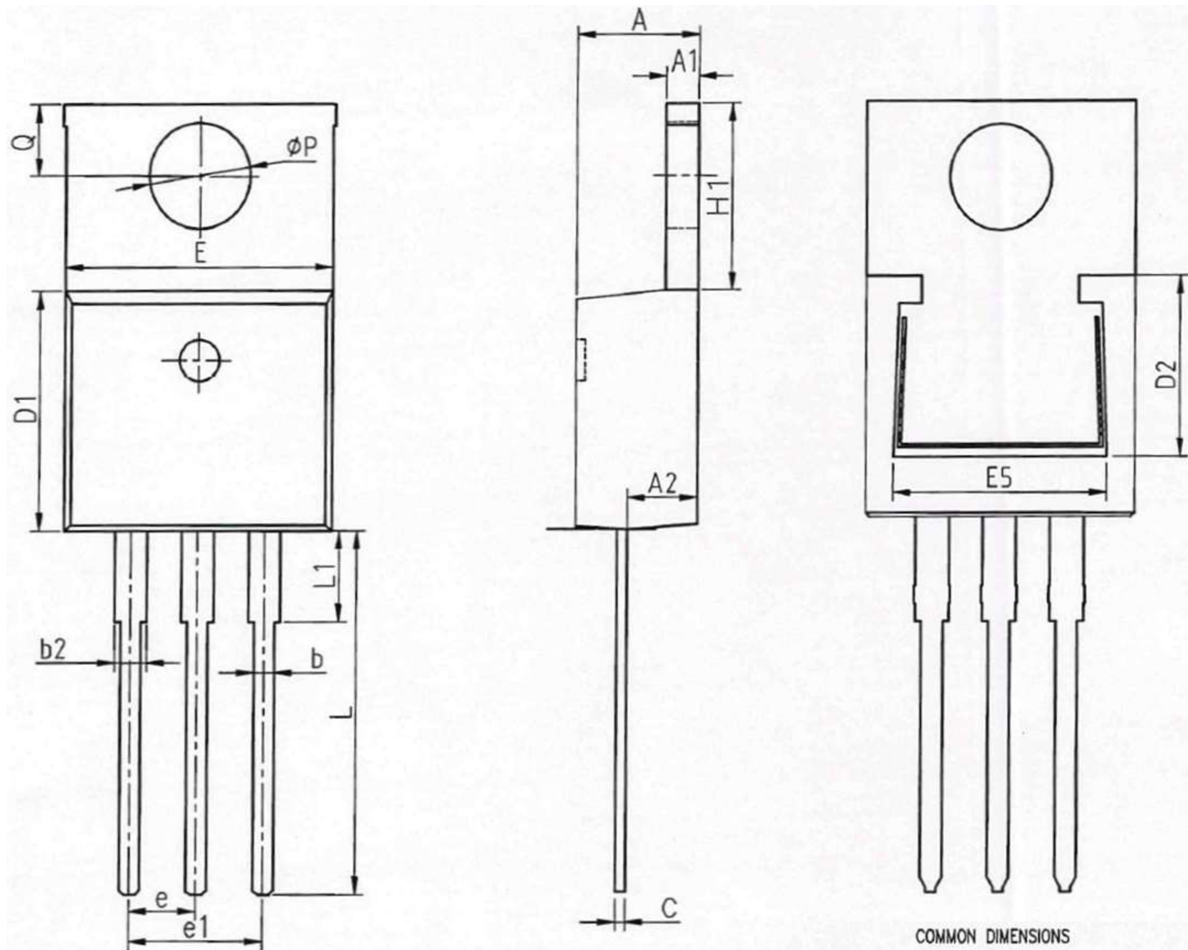

Capacitance
10000
1000
100
10
1
C - Capacitance (pF)
Ciss
Coss
Crss
0
50
100
150
200
VDS - Drain-to-Source Voltage (V)


Source-Drain Diode Forward Voltage
100
10
1
Is - Source Current (A)
TJ = 125˚C
TJ = 25˚C
0
0.2
0.4
0.6
0.8
1
1.2
1.4
VSD - Source-to-Drain Voltage (V)


Maximum Rated Forward Biased Safe Operating Area
RDS(on) Limited
VGS=10V
TA = 25ºC,
Single Pulse
10µs
100µs
1ms
10ms
DC
RDS(on) Limit
Package Limit
Thermal Limit
100
10
1
0.1
0.01
ID - Drain Current (A)
0.1
1
10
100
1000
VDS - Drain-to-Source Voltage (V)


Transient Thermal Response, Junction-to-Ambient
1
0.1
0.01
0.001
0.50
0.20
0.10
0.05
0.02
Single Pulse
r(t) - Transient Thermal Resistance (Normalized)
Notes:
PDM
t1
t2
1. Duty Cycle, D = t1/t2
1.0E-06
1.0E-05
1.0E-04
1.0E-03
1.0E-02
1.0E-01
1.0E+00
t - Time (seconds)

Package Outline: TO-220



SYMBOL	MM		
	MIN	NOM	MAX
A	4.37	4.57	4.77
A1	1.22	1.27	1.40
A2	2.49	2.69	2.89
b	0.75	0.81	0.96
b2	1.22	1.27	1.47
c	0.30	0.38	0.48
D1	8.50	8.70	8.90
D2	5.20	-	-
E	9.86	10.16	10.36
E5	7.06	-	-
e	2.54 BSC		
e1	5.08 BSC		
H1	6.10	6.30	6.50
L	13.10	13.40	13.70
L1	-	3.75	4.10
ΦP	3.70	3.84	3.99
Q	2.54	2.74	2.94

ICEMOS SUPERJUNCTION PATENT PORTFOLIO

ICEMOS GRANTED PATENTS

US7,429,772
US7,439,178
US7,446,018
US7,579,607
US7,723,172
US7,795,045
US7,846,821
US7,944,018
US8,012,806
US8,030,133

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US7,023,069B2
US7,364,994
US7,227,197B2
US7,304,944B2
US7,052,982B2
US7,339,252
US7,410,891
US7,439,583
US7,227,197B2
US6,635,906
US6,936,867
US7,015,104
US9,109,110
US7,271,067
US7,354,818
US7,052,982,
US7,199,006B2

Note: additional patents in China, Korea, Japan, Taiwan, Europe have also been granted to IceMOS and 3D Semi for Superjunction MOSFETs with 70 additional Patent applications in process in the USA and the above listed countries.

Marking Information

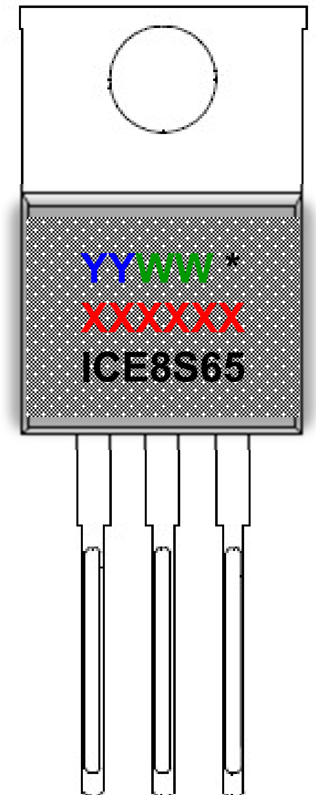
YY = Last two digits of the year

WW = Work week

* = Site ID

XXXXXX = Lot ID

ICE8S65 = ICE is IceMOS logo and
8S65 is a designated device part number



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