ICE8S65FP N-Channel Enhancement Mode MOSFET

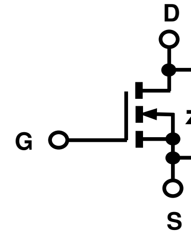
RoHS compliant 2011/65/EU

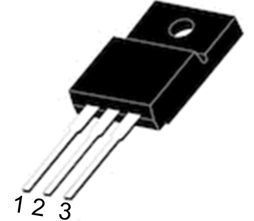
HALOGEN FREE

Product Summary			
I_D	T_A=25°C	8A	Max
BV_{DSS}	I_D=250uA	650V	Min
$r_{DS(on)}$	V_{GS}=10V	0.36Ω	Typ
Q_g	V_{DS}=480V	11.5nC	Typ

Features

- Low $r_{DS(on)}$
- Ultra Low Gate Charge
- High d*v*/d*t* capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Optimized design for hard switching SMPS topologies





T0220FP

Isolated (T0-220)

1=Gate, 2=Drain, 3=Source.

ICEMOS AND ITS SISTER COMPANY 3D SEMI OWN THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 to 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN & EUROPE.

Maximum ratings at T_j=25°C, unless otherwise specified

Parameter	*Symbol*	*Conditions*	*Value*	*Unit*
Continuous drain current	I_D	T_c=25°C T_c=100°C	8 5.0	A
Pulsed drain current	$I_{D,\ pulse}$	T_c=25°C	18	A
Avalanche energy, single pulse	E_{AS}	I_D=2.7A	40	mJ
Avalanche current, repetitive	I_{AR}	limited by $T_j$max	2.7	A
MOSFET d*v*/d*t* ruggedness	d*v*/d*t*	V_{DS}=480V, I_D=8A, T_j=125°C	50.0	V/ns
Gate source voltage	V_{GS}	Static	±20	V
		AC (*f*>1Hz)	±30	
Power dissipation	P_{tot}	T_c=25°C	35	W
Operating and storage temperature	T_j, T_{stg}		-55 to +150	°C

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

Thermal characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Thermal resistance, junction-case [a]	R_{thJC}		-	-	3.5	°C/W
Thermal resistance, junction-ambient [a]	R_{thJA}	leaded	-	-	62	
Soldering temperature, wave soldering only allowed at leads	T_{sold}	1.6mm (0.063in.) from case for 10 s	-	-	260	°C

Electrical characteristics at T_j=25°C, unless otherwise specified

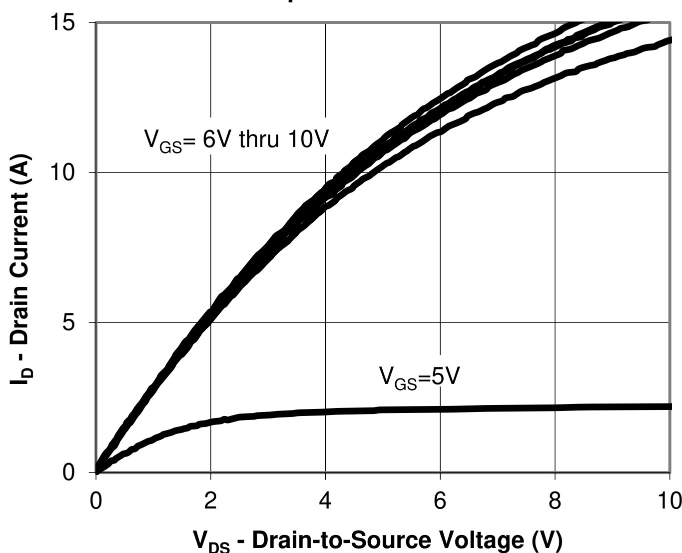
Static characteristics

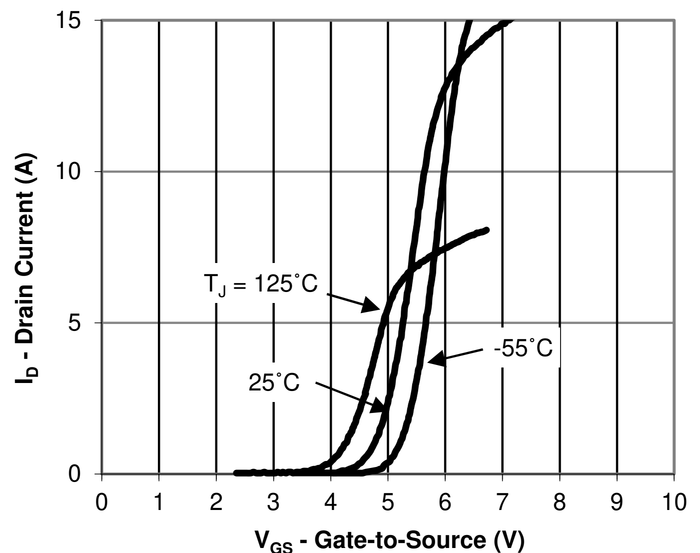
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=250μA	650	700	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	2.1	3	3.9	
Zero gate voltage drain current	I_{DSS}	V_{DS}=650V, V_{GS}=0V, T_j=25°C	-	0.1	1	μA
		V_{DS}=650V, V_{GS}=0V, T_j=150°C	-	100	-	
Gate source leakage current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0V	-	-	100	nA
Drain-source on-state resistance	$r_{DS(on)}$	V_{GS}=10V, I_D=4A, T_j=25°C	-	0.36	0.40	Ω
		V_{GS}=10V, I_D=4A, T_j=150°C	-	1.01	-	
Gate resistance	R_G	f=1 MHZ, open drain	-	2	-	Ω

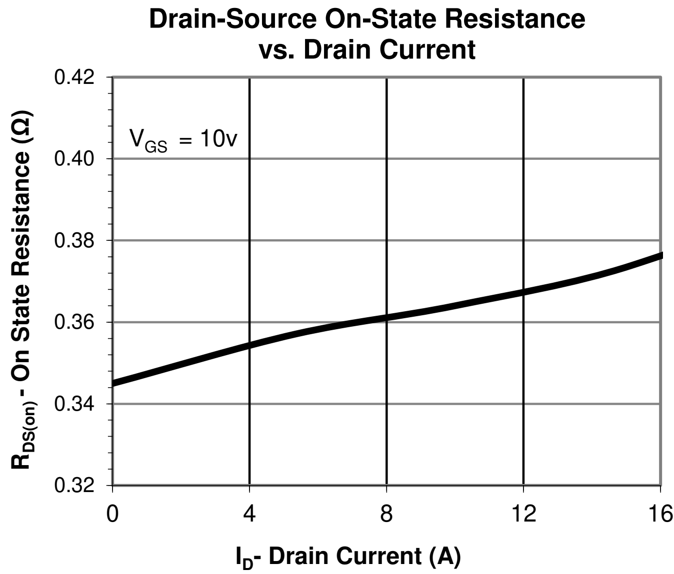
Dynamic characteristics

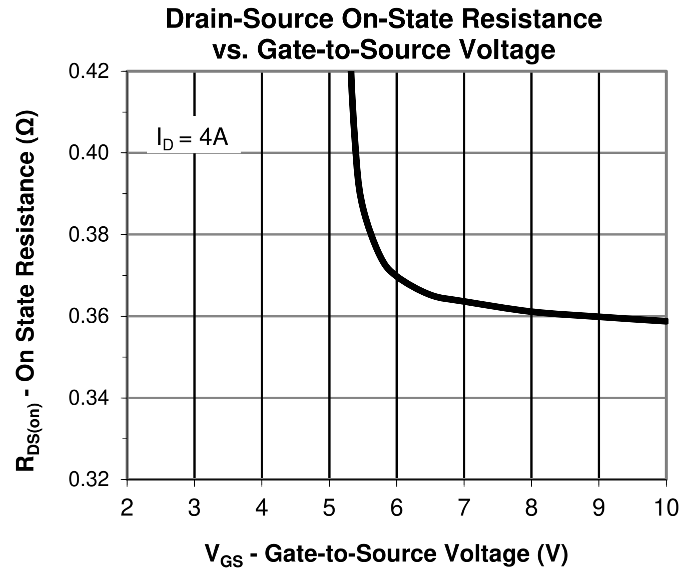
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=25V, f=1 MHz	-	520	-	pF
Output capacitance	C_{oss}		-	67	-	
Reverse transfer capacitance	C_{rss}		-	1	-	
Output capacitance	C_{oss}	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz	-	22	-	
Transconductance	g_{fs}	V_{DS}>2*I_D*R_{DS}, I_D=4A	-	8	-	S
Turn-on delay time	$t_{d(on)}$	V_{DS}=380V, V_{GS}=10V, I_D=8A, R_G=4Ω (External)	-	16	-	ns
Rise time	t_r		-	41	-	
Turn-off delay time	$t_{d(off)}$		-	28	-	
Fall time	t_f		-	23	-	

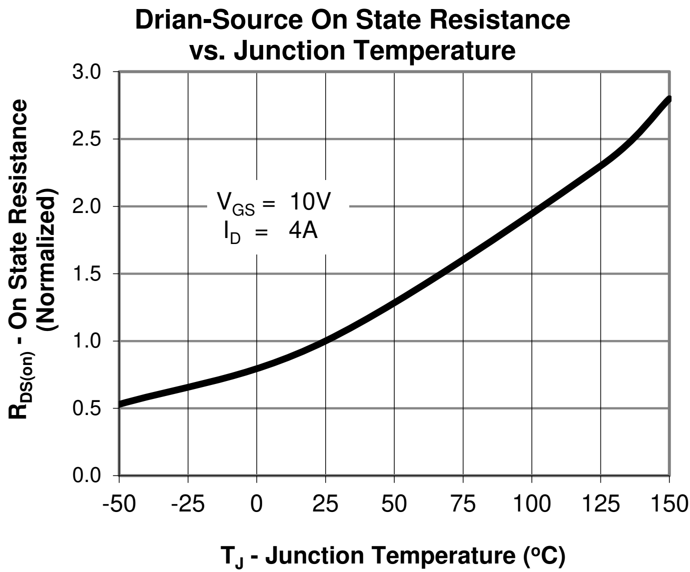
Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Gate charge characteristics						
Gate to source charge	Q_{gs}	V_{DS}=480 V, I_D=10A, V_{GS}=8 V	-	2.9	-	nC
Gate to drain charge	Q_{gd}		-	2.5	-	nC
Gate charge total	Q_g		-	11.5	-	nC
Gate plateau voltage	$V_{plateau}$		-	5.5	-	V
Reverse Diode						
Continuous forward current	I_S	V_{GS}=0V	-	-	8	A
Diode forward voltage	V_{SD}	V_{GS}=0V, I_S=I_F	-	1.0	1.2	V
Reverse recovery time	t_{rr}	V_{RR}=50V, I_S=I_F, d_{iF}/d_t=100 A/µS	-	330	-	ns
Reverse recovery charge	Q_{rr}		-	5	-	µC
Peak reverse recovery current	I_{rm}		-	23	-	A

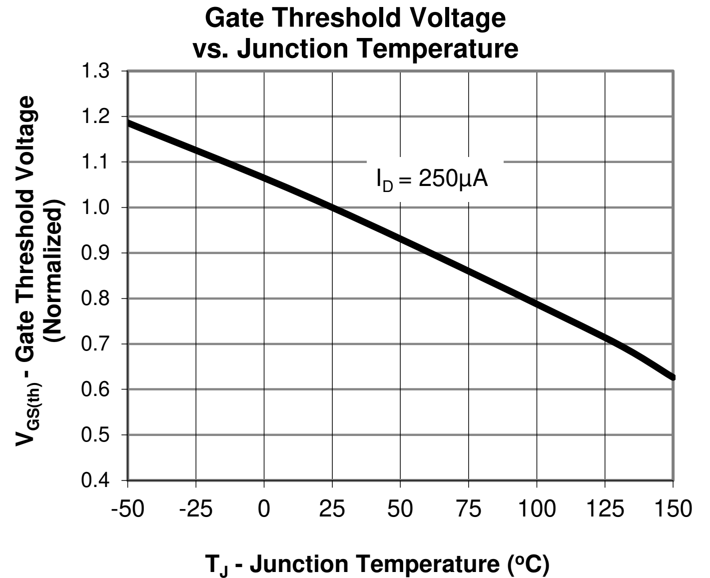


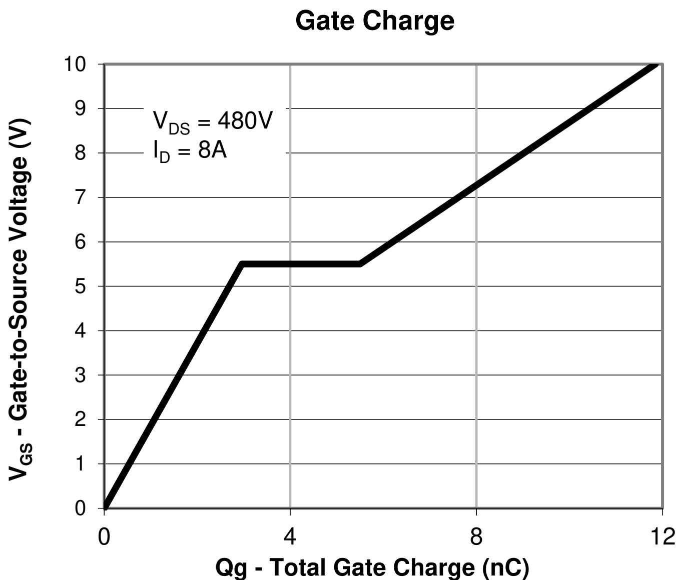


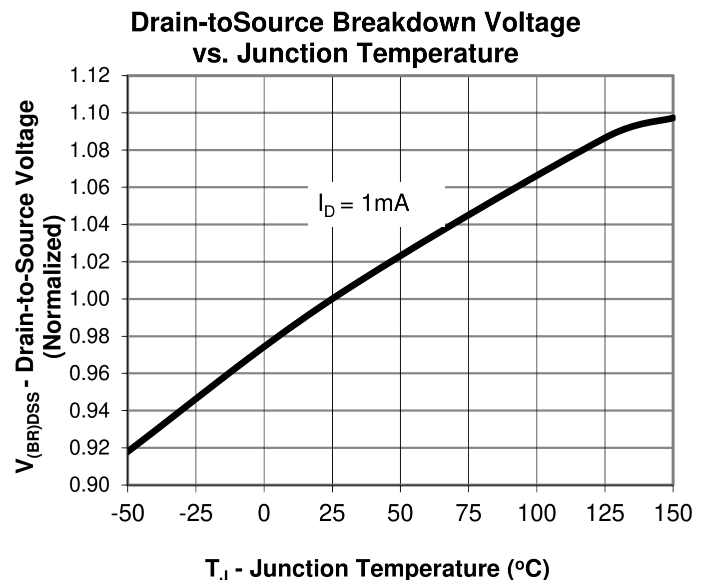

Drain-Source On-State Resistance
vs. Drain Current
V_GS = 10v
R_DS(on) - On State Resistance (Ω)
I_D- Drain Current (A)
0.42
0.40
0.38
0.36
0.34
0.32
0
4
8
12
16

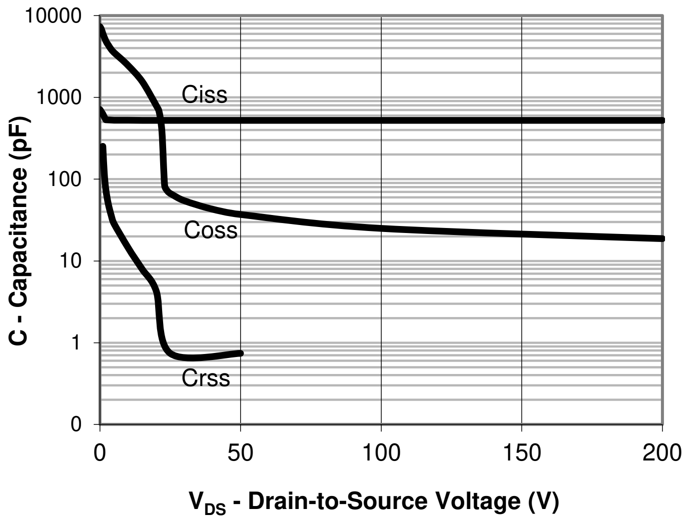

Drain-Source On-State Resistance
vs. Gate-to-Source Voltage
I_D = 4A
R_DS(on) - On State Resistance (Ω)
V_GS - Gate-to-Source Voltage (V)
0.42
0.40
0.38
0.36
0.34
0.32
2
3
4
5
6
7
8
9
10

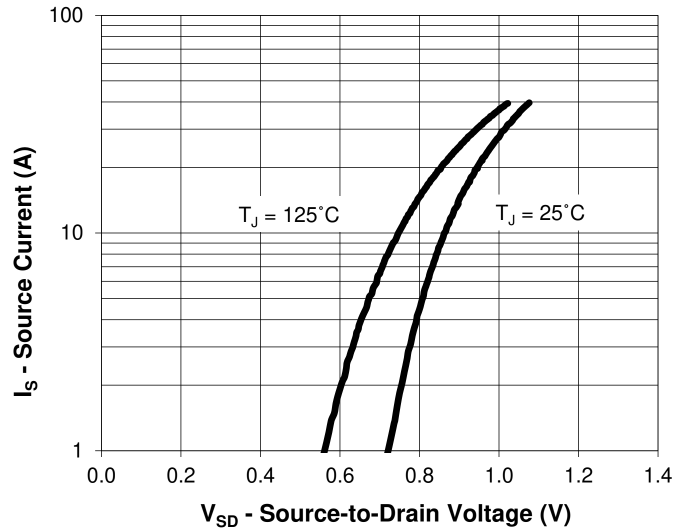

Drian-Source On State Resistance
vs. Junction Temperature
V_GS = 10V
I_D = 4A
R_DS(on) - On State Resistance
(Normalized)
T_J - Junction Temperature (°C)
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-50
-25
0
25
50
75
100
125
150

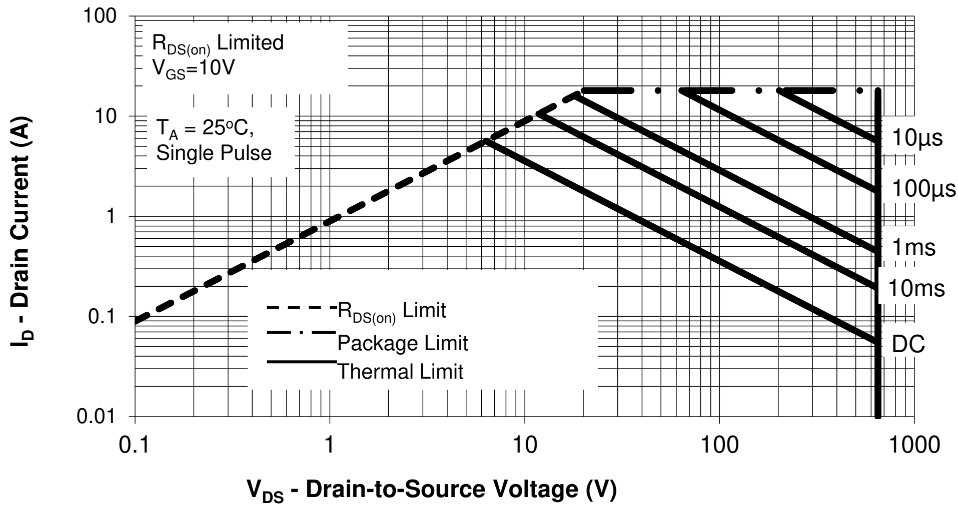

Gate Threshold Voltage
vs. Junction Temperature
I_D = 250µA
V_GS(th) - Gate Threshold Voltage
(Normalized)
T_J - Junction Temperature (°C)
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
-50
-25
0
25
50
75
100
125
150

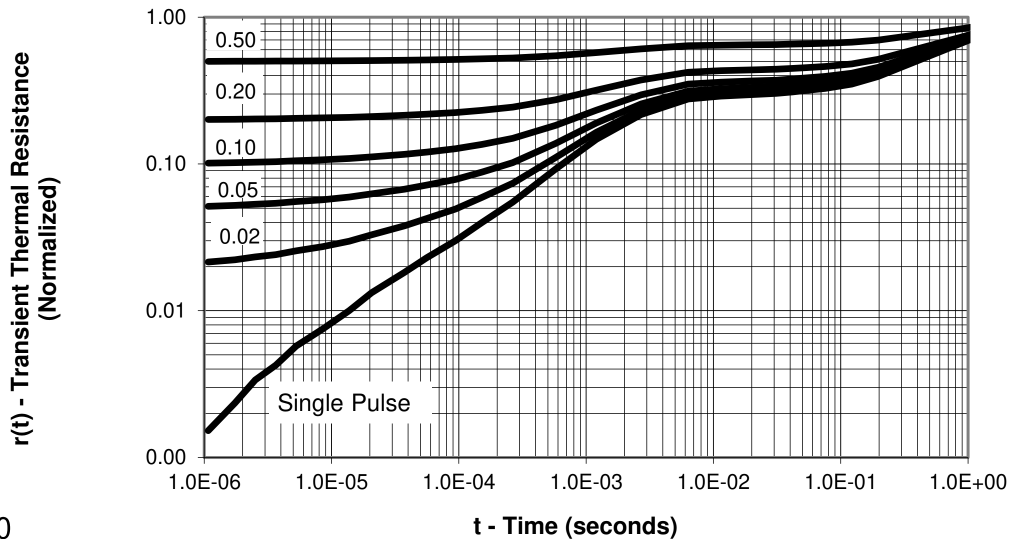

Gate Charge
V_DS = 480V
I_D = 8A
V_GS - Gate-to-Source Voltage (V)
Qg - Total Gate Charge (nC)
10
9
8
7
6
5
4
3
2
1
0
0
4
8
12


Drain-toSource Breakdown Voltage
vs. Junction Temperature
I_D = 1mA
V_(BR)DSS - Drain-to-Source Voltage
(Normalized)
T_J - Junction Temperature (°C)
1.12
1.10
1.08
1.06
1.04
1.02
1.00
0.98
0.96
0.94
0.92
0.90
-50
-25
0
25
50
75
100
125
150

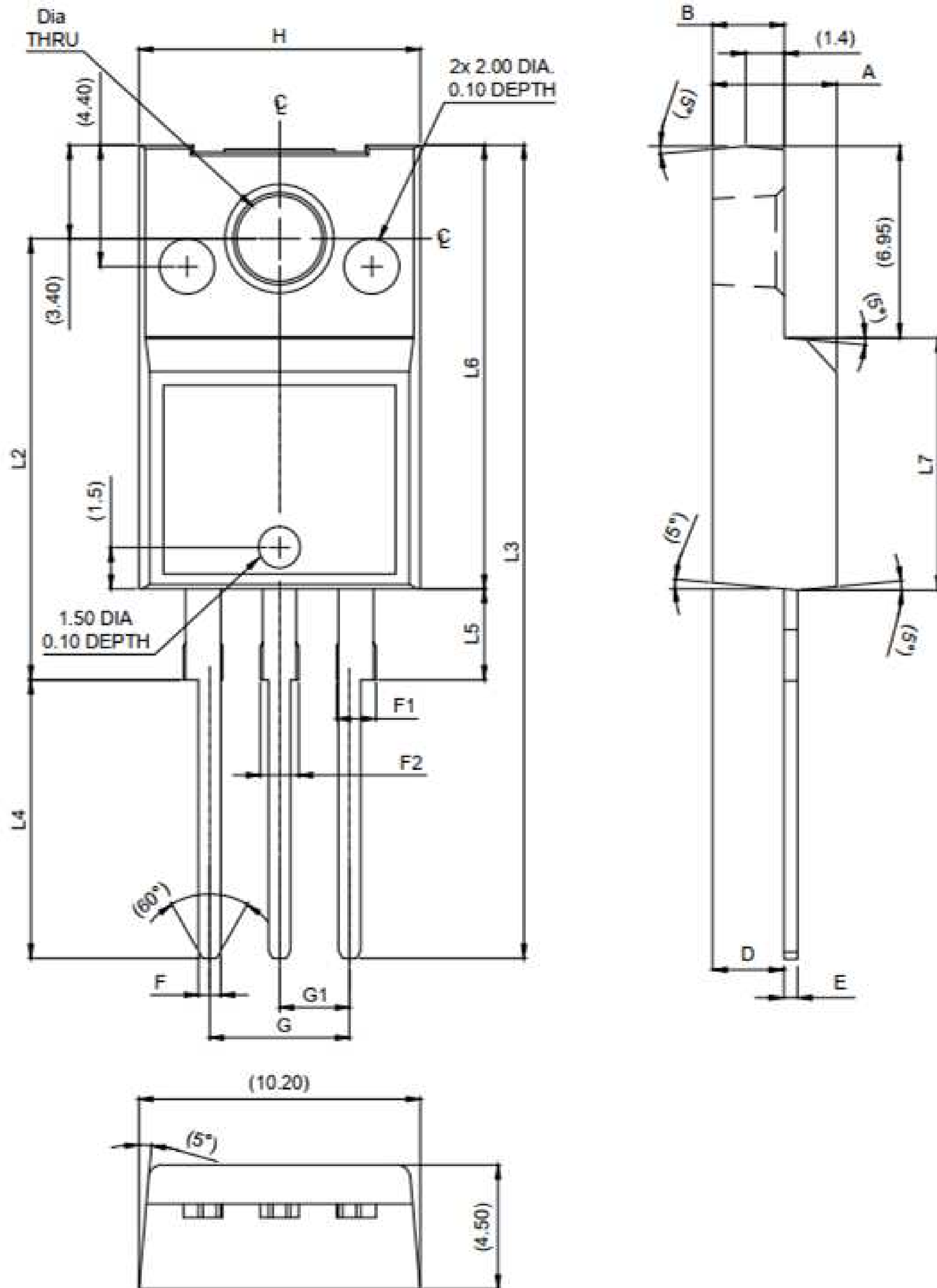

Capacitance
10000
1000
100
10
1
0
Ciss
Coss
Crss
0
50
100
150
200
C - Capacitance (pF)
VDS - Drain-to-Source Voltage (V)


Source-Drain Diode Forward Voltage
100
10
1
TJ = 125˚C
TJ = 25˚C
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
IS - Source Current (A)
VSD - Source-to-Drain Voltage (V)


Full Pak TO-220 Package
Maximum Rated Forward Biased SOA
RDS(on) Limited
VGS=10V
TA = 25ºC,
Single Pulse
10µs
100µs
1ms
10ms
DC
RDS(on) Limit
Package Limit
Thermal Limit
100
10
1
0.1
0.01
0.1
1
10
100
1000
ID - Drain Current (A)
VDS - Drain-to-Source Voltage (V)


Transient Thermal Response, Junction-to-Ambient
1.00
0.10
0.01
0.00
0.50
0.20
0.10
0.05
0.02
Single Pulse
1.0E-06
1.0E-05
1.0E-04
1.0E-03
1.0E-02
1.0E-01
1.0E+00
r(t) - Transient Thermal Resistance
(Normalized)
t - Time (seconds)

Package Outline: TO-220 FullPAK



Package Outline: TO-220 FullPAK

SYMBOL	MIN	NOM	MAX	NOTES
A	4.4		4.6	1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
B	2.5		2.7	2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
D	2.5		2.75	
E	0.45		0.7	
F	0.75		1	
F1	1.15		1.5	
F2	1.15		1.5	
G	4.95		5.2	
G1	2.4		2.7	
H	10		10.4	
L2		16		
L3	28.6		30.6	
L4	9.8		10.6	
L5	2.9		3.6	
L6	15.9		16.4	
L7	9		9.3	
Dia	3		3.2	

ICEMOS SUPERJUNCTION PATENT PORTFOLIO

ICEMOS GRANTED PATENTS

US7,429,772
US7,439,178
US7,446,018
US7,579,607
US7,723,172
US7,795,045
US7,846,821
US7,944,018
US8,012,806
US8,030,133

3D SEMI PATENTS LICENSED TO ICEMOS

US7,041,560B2
US7,023,069B2
US7,364,994
US7,227,197B2
US7,304,944B2
US7,052,982B2
US7,339,252
US7,410,891
US7,439,583
US7,227,197B2
US6,635,906
US6,936,867
US7,015,104
US9,109,110
US7,271,067
US7,354,818
US7,052,982,
US7,199,006B2

Note: additional patents in China, Korea, Japan, Taiwan, Europe have also been granted to IceMOS and 3D Semi for Superjunction MOSFETs with 70 additional Patent applications in process in the USA and the above listed countries.

Marking Information

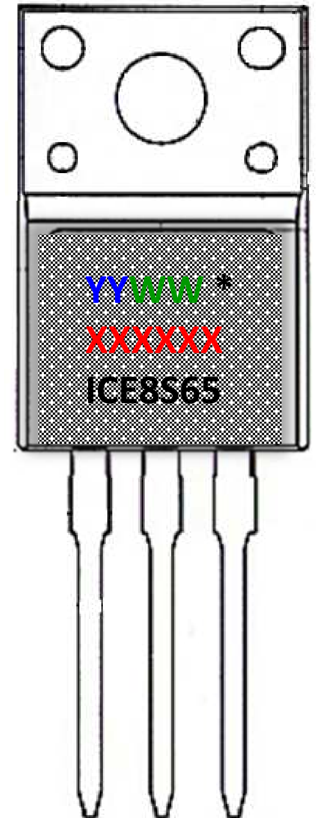
YY = Last two digits of the year

WW = Work week

* = Site ID

XXXXXX = Lot ID

ICE8S65 = ICE is IceMOS logo and
8S65 is a designated device part number



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