

### ICE17N60 N-Channel Enhancement Mode MOSFET

RoHS compliant  
2011/65/EU



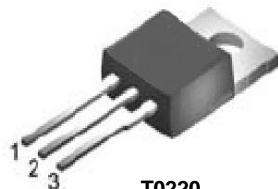
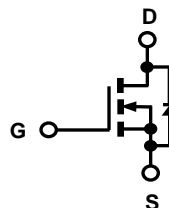
HALOGEN FREE

Product Summary			
$I_D$	$T_A=25^\circ\text{C}$	17A	Max
$V_{(BR)DSS}$	$I_D=250\mu\text{A}$	600V	Min
$r_{DS(on)}$	$V_{GS}=10\text{V}$	0.19 $\Omega$	Typ
$Q_g$	$V_{DS}=480\text{V}$	59nC	Typ

#### Features

- Low  $r_{DS(on)}$
- Ultra Low Gate Charge
- High  $dv/dt$  capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems

ICEMOS AND ITS SISTER COMPANY 3D SEMI OWN THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 TO 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN & EUROPE.



TO220

Standard Metal Heatsink

1=Gate, 2=Drain, 3=Source.

**Maximum ratings**<sup>b</sup>, at  $T_j=25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$T_c=25^\circ\text{C}$	17	A
Pulsed drain current	$I_{D, pulse}$	$T_c=25^\circ\text{C}$	51	A
Avalanche energy, single pulse	$E_{AS}$	$I_D=8.5\text{A}$	460	mJ
Avalanche current, repetitive	$I_{AR}$	limited by $T_{jmax}$	8.5	A
MOSFET $dv/dt$ ruggedness	$dv/dt$	$V_{DS}=480\text{V}$ , $I_D=17\text{A}$ , $T_j=125^\circ\text{C}$	50	V/ns
Gate source voltage	$V_{GS}$	Static	$\pm 20$	V
		AC ( $f > 1\text{Hz}$ )	$\pm 30$	
Power dissipation	$P_{tot}$	$T_c=25^\circ\text{C}$	186	W
Operating and storage temperature	$T_j, T_{stg}$		-55 to +150	$^\circ\text{C}$
Mounting torque		M 3 & 3.5 screws	60	Ncm

a When mounted on 1inch square 2oz copper clad FR-4

b Preliminary Data Sheet – Specifications subject to change

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

### Thermal characteristics

Thermal resistance, junction-case <sup>a</sup>	$R_{thJC}$		-	-	0.8	°C/W
Thermal resistance, junction-ambient <sup>a</sup>	$R_{thJA}$	leaded	-	-	62	
Soldering temperature, wave soldering only allowed at leads	$T_{sold}$	1.6mm (0.063in.) from case for 10 s	-	-	260	°C

### Electrical characteristics <sup>b</sup>, at $T_j=25^\circ\text{C}$ , unless otherwise specified

#### Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=250\mu\text{A}$	600	640	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.1	3	3.9	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=600\text{V}, V_{GS}=0\text{V}, T_j=25^\circ\text{C}$	-	0.1	1	$\mu\text{A}$
		$V_{DS}=600\text{V}, V_{GS}=0\text{V}, T_j=150^\circ\text{C}$	-	-	100	
Gate source leakage current	$I_{GSS}$	$V_{GS}=\pm 20\text{ V}, V_{DS}=0\text{V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=8.5\text{A}, T_j=25^\circ\text{C}$	-	0.19	0.22	$\Omega$
		$V_{GS}=10\text{V}, I_D=8.5\text{A}, T_j=150^\circ\text{C}$	-	0.5	-	
Gate resistance	$R_G$	$f=1\text{ MHz}, \text{open drain}$	-	4.7	-	$\Omega$

#### Dynamic characteristics

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V}, f=1\text{ MHz}$	-	1800	-	$\mu\text{F}$
Output capacitance	$C_{oss}$		-	600	-	
Reverse transfer capacitance	$C_{rss}$		-	5	-	
Transconductance	$g_{fs}$	$V_{DS}>2 * I_D * R_{DS}, I_D=8.5\text{A}$	-	15	-	S
Turn-on delay time	$t_{d(on)}$	$V_{DS}=380\text{V}, V_{GS}=10\text{V}, I_D=17\text{A}, R_G=4\Omega \text{ (External)}$	-	39	-	ns
Rise time	$t_r$		-	10	-	
Turn-off delay time	$t_{d(off)}$		-	55	-	
Fall time	$t_f$		-	6	-	

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

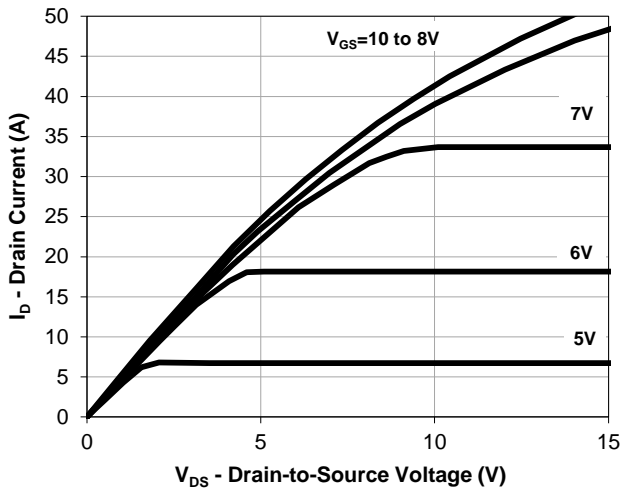
### Gate charge characteristics

Gate to source charge	$Q_{gs}$	$V_{DS}=480\text{ V}, I_D=17\text{ A},$ $V_{GS}=10\text{ V}$	-	11	-	nC
Gate to drain charge	$Q_{gd}$		-	18	-	
Gate charge total	$Q_g$		-	59	-	
Gate plateau voltage	$V_{\text{plateau}}$		-	5.5	-	V

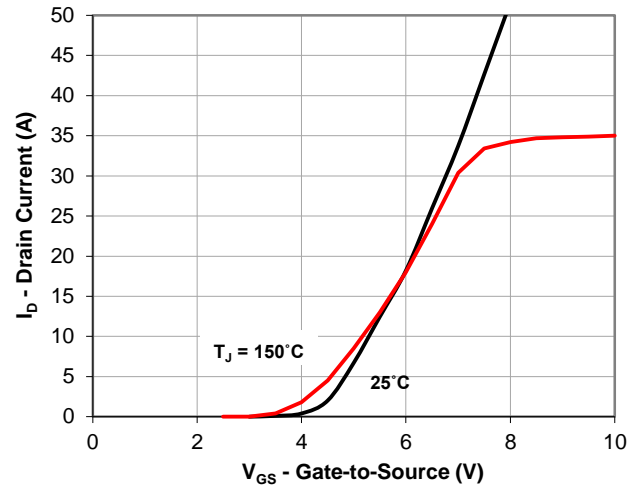
### Reverse Diode

Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_S=I_F$	-	0.9	1.2	V
Reverse recovery time	$t_{rr}$	$V_{RR}=480\text{ V}, I_S=I_F,$ $d_{iF}/d_t=100\text{ A}/\mu\text{S}$	-	400	-	ns
Reverse recovery charge	$Q_{rr}$		-	6	-	$\mu\text{C}$
Peak reverse recovery current	$I_{rm}$		-	35	-	A

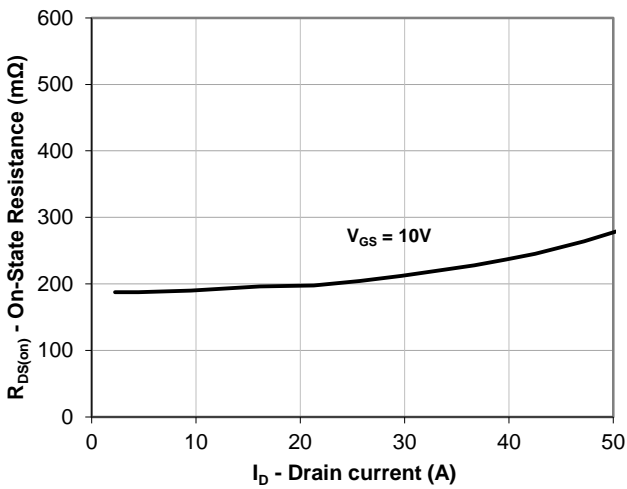
### Output Characteristics



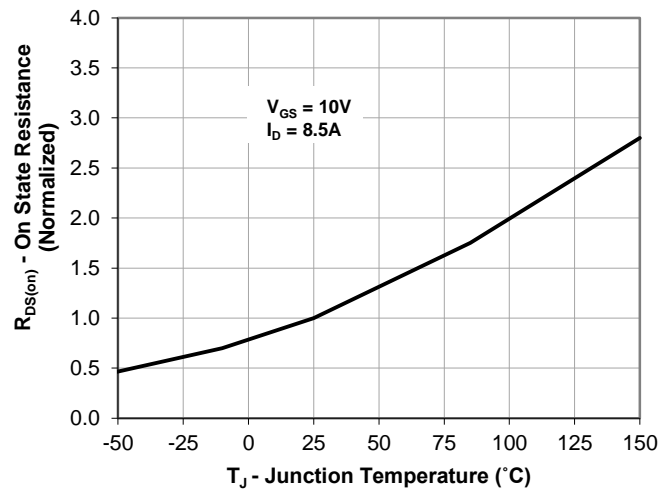
### Transfer Characteristics



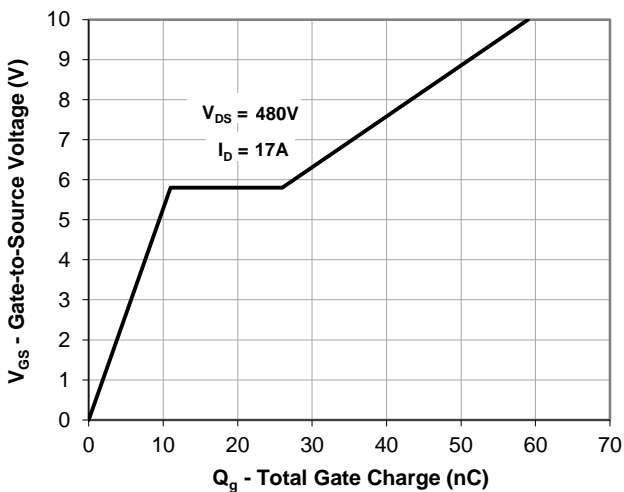
### On Resistance vs Drain Current



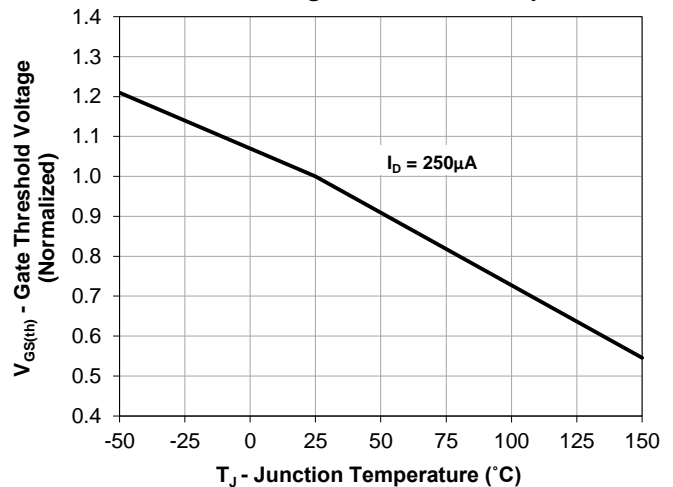
### On Resistance vs Junction Temperature

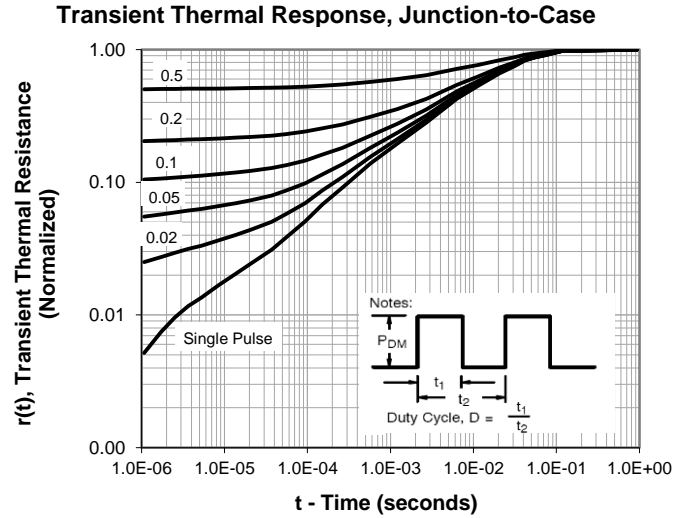
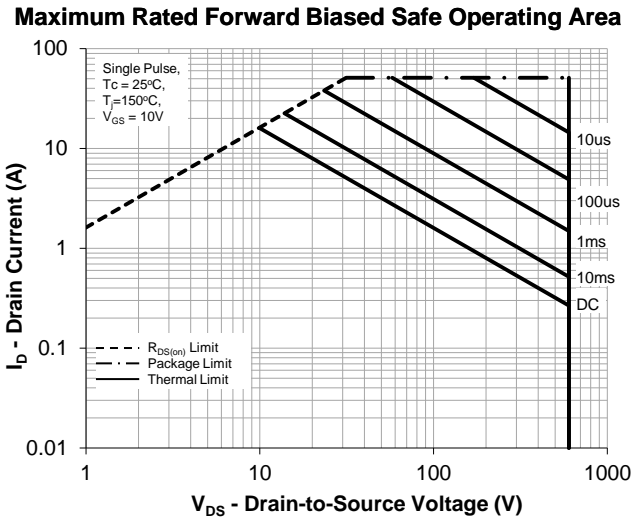
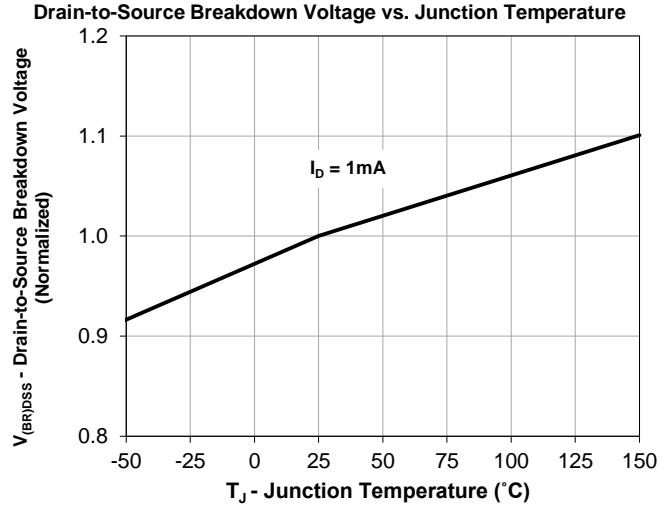
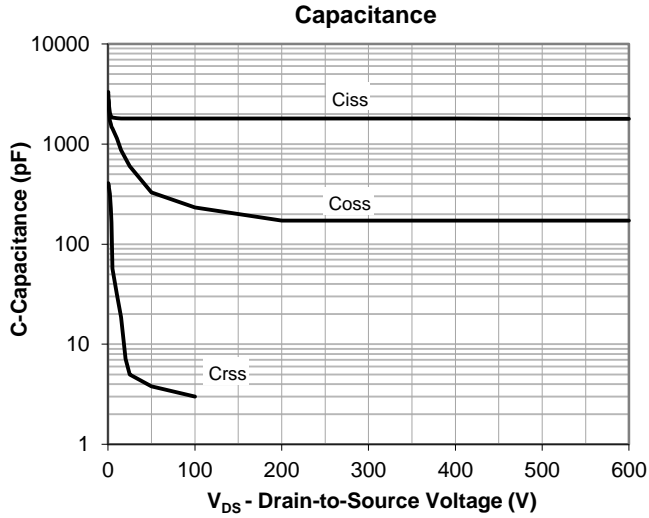


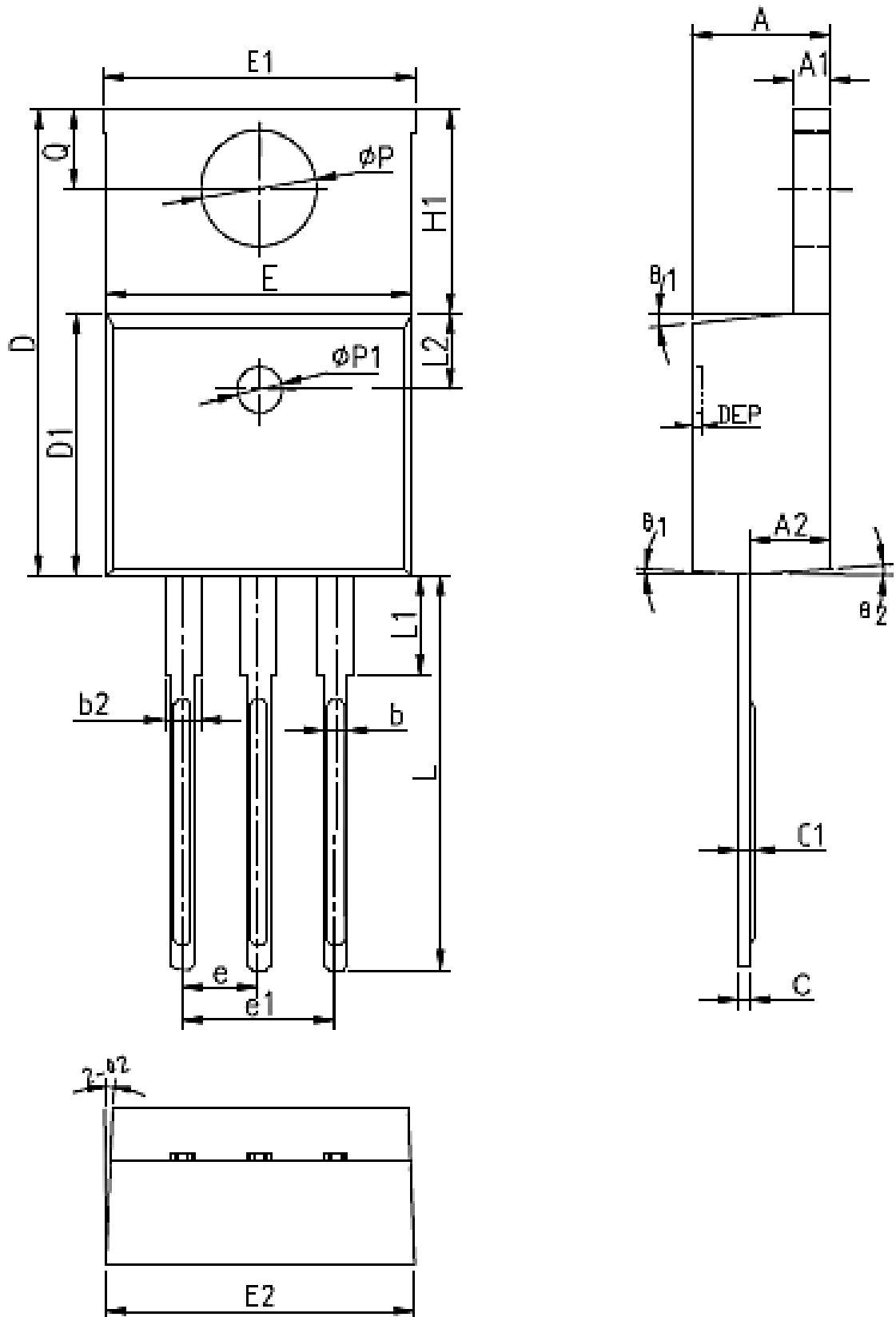
### Gate Charge



### Gate Threshold Voltage vs Junction Temperature







**COMMON DIMENSIONS**

SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.556	4.191	4.826	0.140	0.165	0.190
A1	0.508	1.397	1.40	0.020	0.055	0.055
A2	2.032	2.476	2.921	0.080	0.097	0.115
b	0.356	0.633	0.91	0.014	0.025	0.036
b2	1.05	1.21	1.37	0.041	0.048	0.054
c	0.31	0.46	0.61	0.012	0.018	0.024
c1	0.33	0.465	0.60	0.013	0.018	0.024
D	14.224	15.367	16.51	0.560	0.605	0.650
D1	8.382	8.816	9.25	0.330	0.347	0.364
E	9.652	10.16	10.668	0.380	0.400	0.420
E1	10.10	10.25	10.35	0.398	0.404	0.407
E2	10.00	10.10	10.20	0.394	0.398	0.402
e	2.54 BSC			0.100 BSC		
e1	5.08 BSC			0.200 BSC		
H1	5.842	6.35	6.858	0.230	0.250	0.270
L	12.70	13.716	14.732	0.500	0.540	0.580
L1	3.56	5.145	6.35	0.140	0.203	0.250
L2	2.50 REF			0.098 REF		
ΦP	3.55	3.72	3.89	0.140	0.146	0.153
Q	2.54	2.997	3.048	0.102	0.108	0.114
θ1	5°	7°	9°	5°	7°	9°
θ2	1°	3°	5°	1°	3°	5°
ΦP1	1.40	1.75	2.10	0.055	0.069	0.083
DEP	0.05	0.10	0.20	0.002	0.004	0.008

## ICEMOS SUPERJUNCTION PATENT PORTFOLIO

### ICEMOS GRANTED PATENTS

US7,429,772  
US7,439,178  
US7,446,018  
US7,579,607  
US7,723,172  
US7,795,045  
US7,846,821  
US7,944,018  
US8,012,806  
US8,030,133

### 3D SEMI PATENTS LICENSED TO ICEMOS

US7,041,560B2  
US7,023,069B2  
US7,364,994  
US7,227,197B2  
US7,304,944B2  
US7,052,982B2  
US7,339,252  
US7,410,891  
US7,439,583  
US7,227,197B2  
US6,635,906  
US6,936,867  
US7,015,104  
US9,109,110  
US7,271,067  
US7,354,818  
US7,052,982,  
US7,199,006B2

Note: additional patents in China, Korea, Japan, Taiwan, Europe have also been granted to IceMOS and 3D Semi for Superjunction MOSFETs with 70 additional Patent applications in process in the USA and the above listed countries.



## Marking Information

**YY** = Last two digits of the year

**WW** = Work week calendar on Icemos subcon assembly & test house

**\*** = Initial for Icemos subcon assembly and test house

**XXXX** = Wafer Lot ID

**00** = may be used for wafer ID in a special case.  
= "00" is used unless specified.

**ICE17N60** = ICE is Icemos logo and 17N60 is a designated device part number

