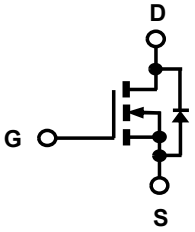
# Preliminary
# ICEK900GL10H8

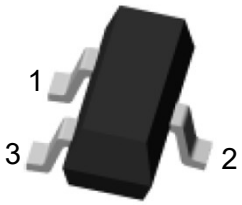
## ICEK900GL10H8 N-Channel Enhancement Mode MOSFET

| Product Summary | | | |
|---|---|---|---|
| $I_D$ | $T_A$=25°C | 2.93A | Max |
| $V_{(BR)DSS}$ | $I_D$=250uA | 100V | Min |
| $r_{DS(on)}$ | $V_{GS}$=10V | 70mΩ | Typ |
| $Q_g$ | $V_{DS}$=50V | 5.4nC | Typ |

### Features

- Low $r_{DS(on)}$
- Superior switching performance
- Optimized design for Motor Drivers and DC-DC Converter




**SOT-23-3L**

**1=Gate, 2=Drain, 3=Source.**

RoHS COMPLIANT RoHS (EU) 2015/863 CE HALOGEN FREE Lead Free

### *Maximum ratings* [a] at $T_j$=25°C, unless otherwise specified

| *Parameter* | *Symbol* | *Conditions* | *Value* | *Unit* |
|---|---|---|---|---|
| Continuous drain current [b] | $I_D$ | $T_c$=25°C | 2.93 | A |
| | | $T_c$=100°C | 1.85 | |
| Pulsed drain current [b] | $I_{D,\ pulse}$ | $T_c$=25°C | 12 | A |
| Avalanche energy, single pulse | $E_{AS}$ | $L$=0.5mH, $V_{DD}$=50V, $I_D$=5.5A, $R_G$=25Ω | 7.5 | mJ |
| Avalanche current, repetitive [b] | $I_{AR}$ | limited by $T_j$max | 5.5 | A |
| Gate source voltage | $V_{GS}$ | Static | ±20 | V |
| | | AC ($f$>1Hz) | | |
| Power dissipation | $P_{tot}$ | $T_c$=25°C | 1.3 | W |
| Operating and storage temperature | $T_j$, $T_{stg}$ | | -55 to +150 | °C |

a Preliminary data sheet - Specifications subject to change.
b limited by $Tj_{max}$
c when mounted on 1-inch square 2oz copper-clad FR-4

| Parameter | Symbol | Conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |

### Thermal characteristics

| | | | | | | |
|---|---|---|---|---|---|---|
| Thermal resistance, junction-ambient [c] | $R_{thJA}$ | leaded | - | - | 95 | °C/W |
| Soldering temperature, wave soldering only allowed at leads | $T_{sold}$ | 1.6mm (0.063in.) from case for 10 s | - | - | 260 | °C |

## Electrical characteristics at $T_j$=25°C, unless otherwise specified

### Static characteristics

| | | | | | | |
|---|---|---|---|---|---|---|
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $V_{GS}$=0V, $I_D$=250µA | 100 | - | - | V |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$, $I_D$=250µA | 1 | 2 | 3 | |
| Zero gate voltage drain current | $I_{DSS}$ | $V_{DS}$=100V, $V_{GS}$=0V | - | - | 1 | µA |
| Gate source leakage current | $I_{GSS}$ | $V_{GS}$=±20V, $V_{DS}$=0V | - | - | ±100 | nA |
| Drain-source on-state resistance | $R_{DS\ (on)}$ | $V_{GS}$=10V, $I_D$=1A | - | 70 | 90 | mΩ |
| Gate resistance | $R_G$ | $f$=1 MHz, open drain | - | 1.1 | - | Ω |

### Dynamic characteristics

| | | | | | | |
|---|---|---|---|---|---|---|
| Input capacitance | $C_{iss}$ | $V_{DS}$=50V, $V_{GS}$=0V, $f$=1 MHz | - | 230 | - | pF |
| Output capacitance | $C_{oss}$ | | - | 70 | - | |
| Reverse transfer capacitance | $C_{rss}$ | | - | 8 | - | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DS}$=15V, $R_L$=7.5Ω, $V_{GS}$=10V, $R_G$=6.8Ω (External) | - | 3 | - | ns |
| Rise time | $t_r$ | | - | 16.5 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 7.5 | - | |
| Fall time | $t_f$ | | - | 3.5 | - | |

| Parameter | Symbol | Conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| ***Gate charge characteristics*** | | | | | | |
| Gate to source charge | $Q_{gs}$ | $V_{DS}$=50V, $I_D$=2A, $V_{GS}$=0 to 10V | - | 0.8 | - | nC |
| Gate to drain charge | $Q_{gd}$ | | - | 1.1 | - | |
| Gate charge total | $Q_g$ | | - | 5.4 | - | |
| ***Reverse Diode*** | | | | | | |
| Continuous forward current | $I_S$ | $V_{GS}$=0V | - | 2.93 | - | A |
| Diode forward voltage | $V_{SD}$ | $V_{GS}$=0V, $I_S$=1A | - | 0.82 | - | V |
| Reverse recovery time | $t_{rr}$ | $V_{RR}$=15V, $I_S$=2A, $d_{iF}/d_t$=100 A/µS | - | 25 | - | ns |
| Reverse recovery charge | $Q_{rr}$ | | - | 13 | - | nC |
| Peak reverse recovery current | $I_{rm}$ | | - | 1 | - | A |

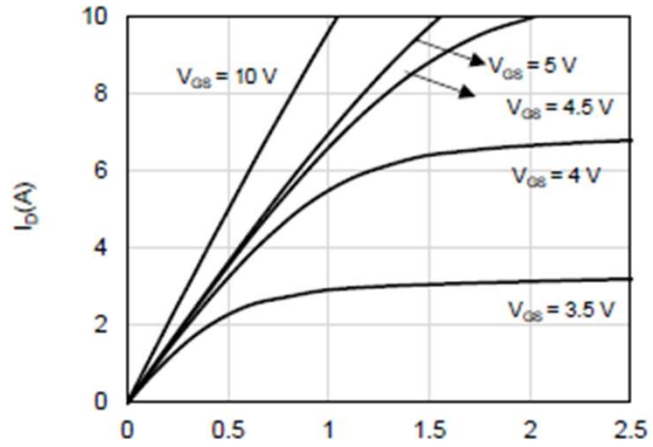



Figure 1: On-Region Characteristics

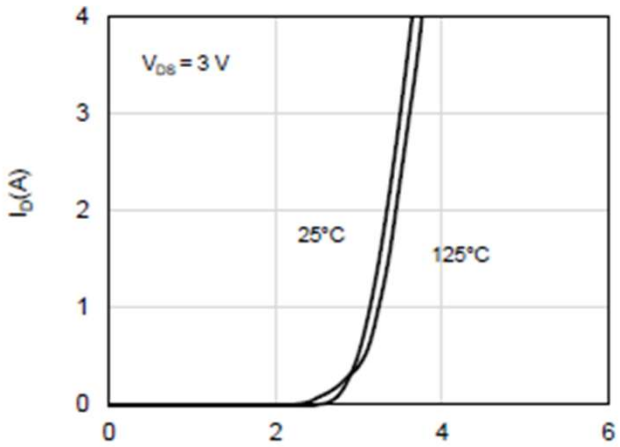



Figure 2: Transfer Characteristics

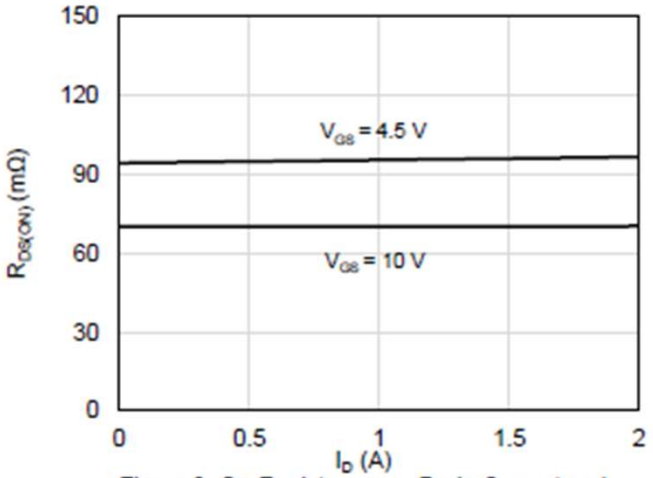



Figure 3: On-Resistance vs. Drain Current and Gate Voltage

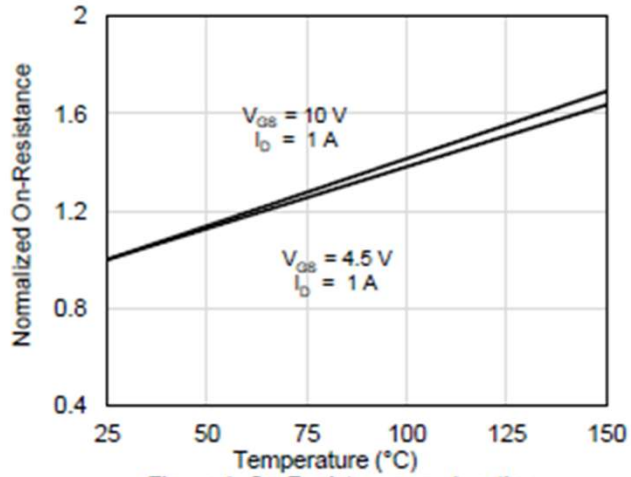



Figure 4: On-Resistance vs. Junction Temperature

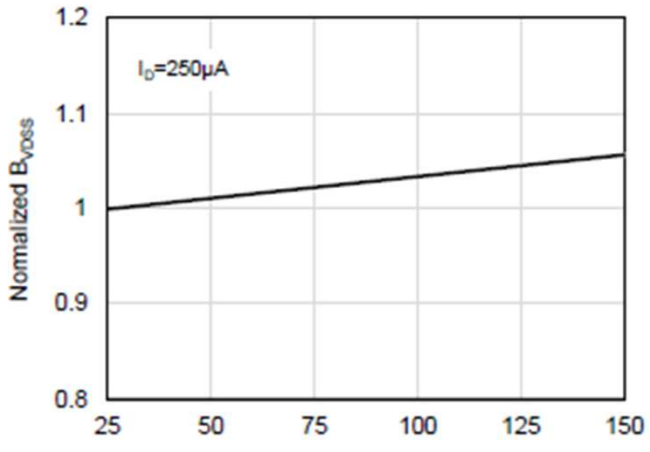



Figure 5: Breakdown Voltage vs. Junction Temperature

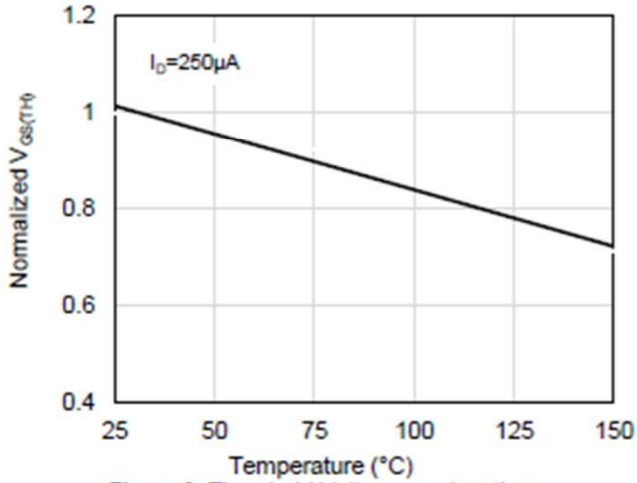



Figure 6: Threshold Voltage vs. Junction Temperature

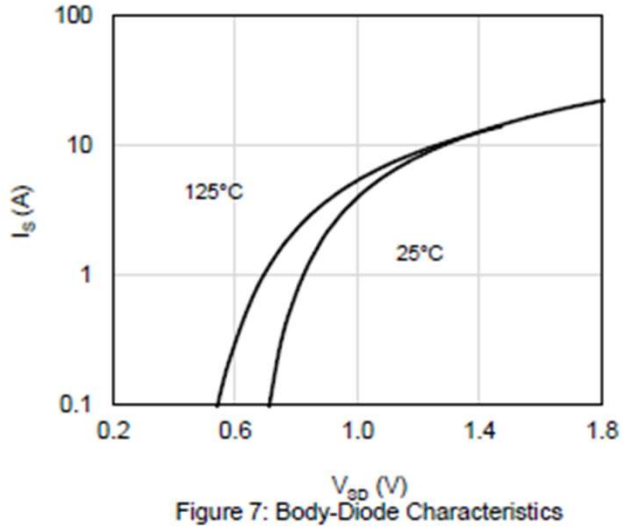


Figure 7: Body-Diode Characteristics

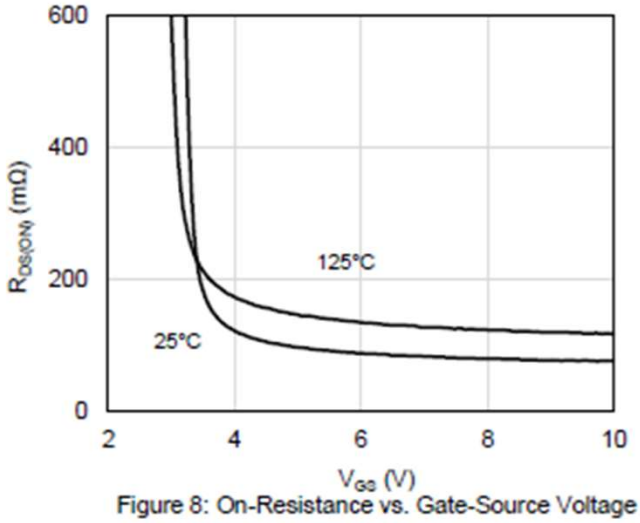


Figure 8: On-Resistance vs. Gate-Source Voltage

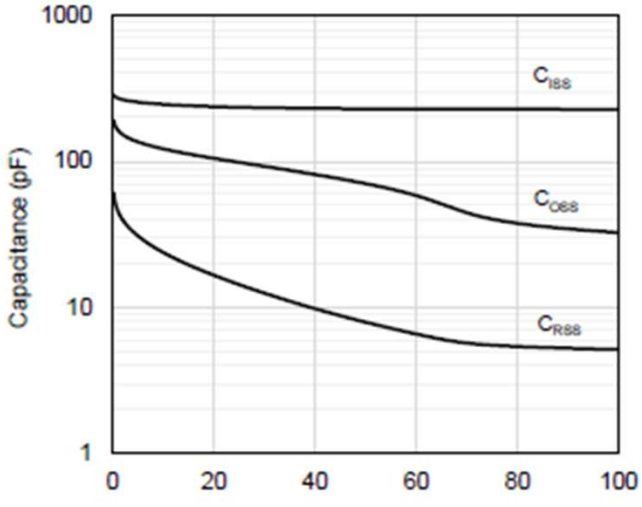


Figure 9: Capacitance Characteristics

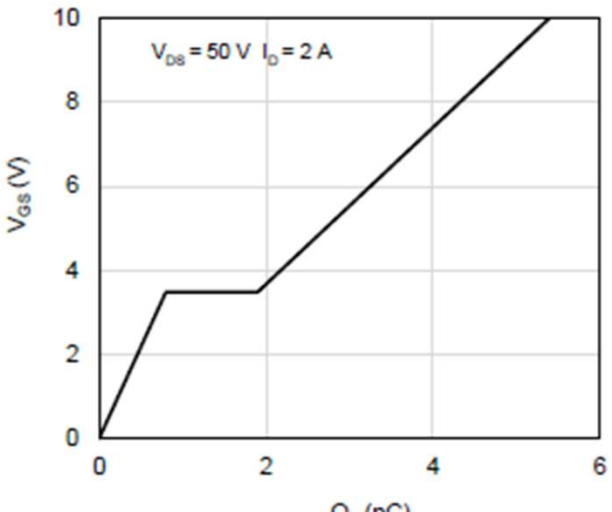


Figure 10: Gate-Charge Characteristics

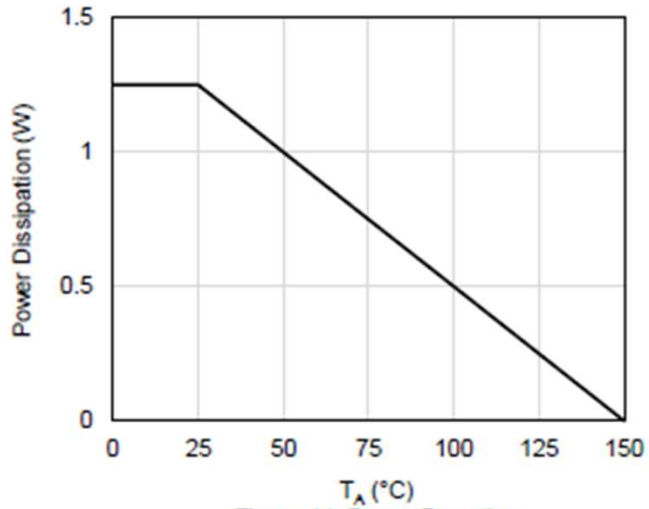


Figure 11: Power De-rating

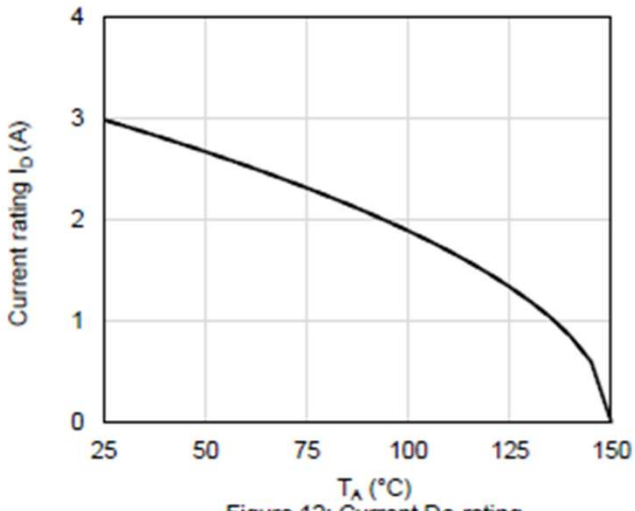


Figure 12: Current De-rating

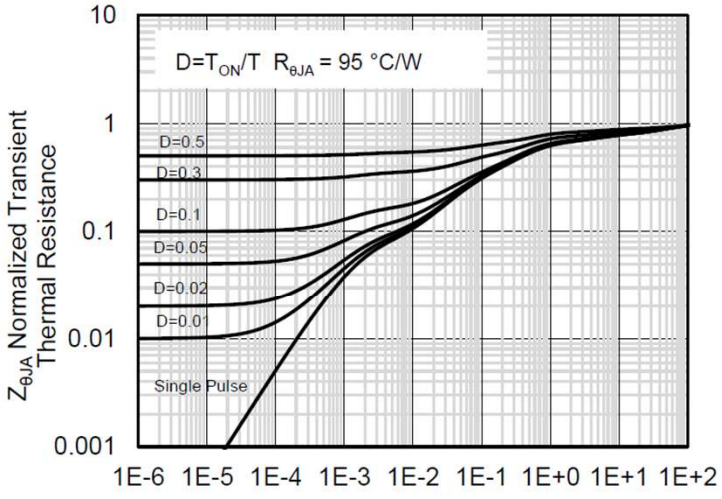



Figure 13: Normalized Maximum Transient Thermal Impedance

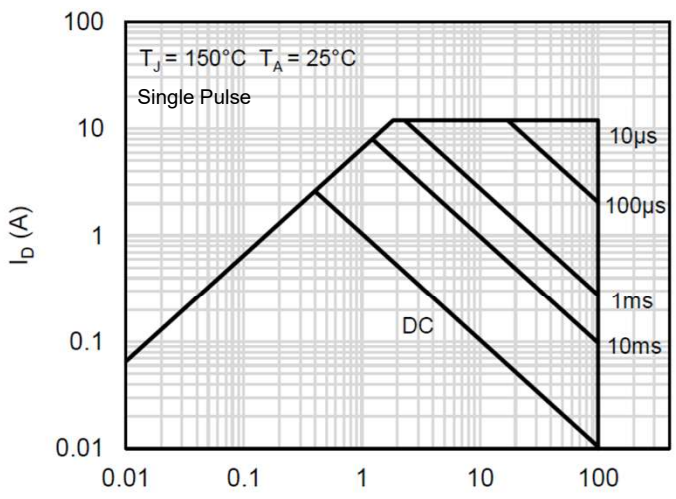
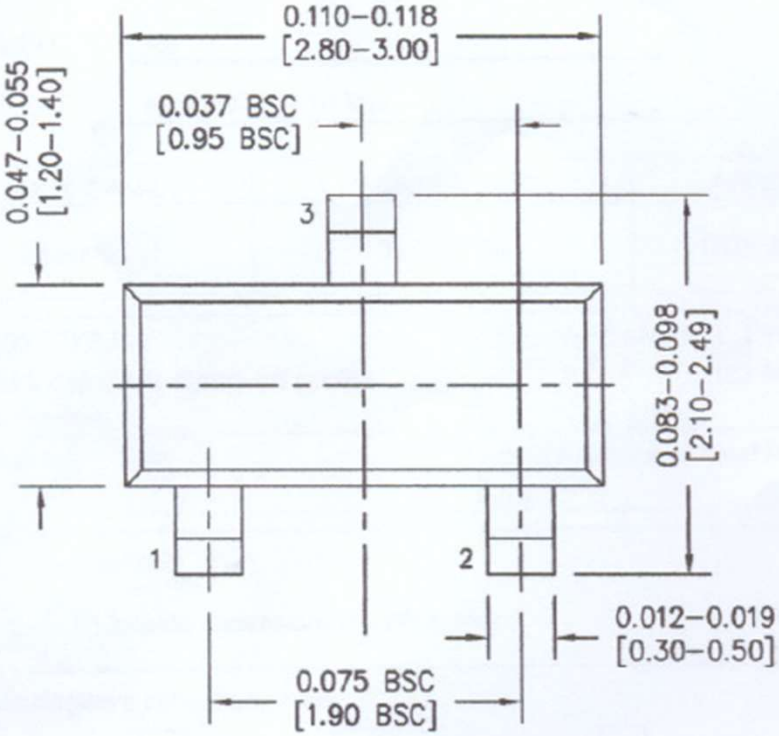
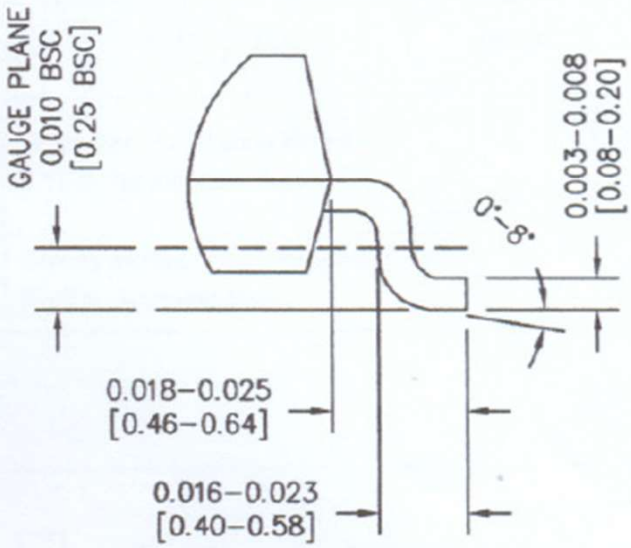


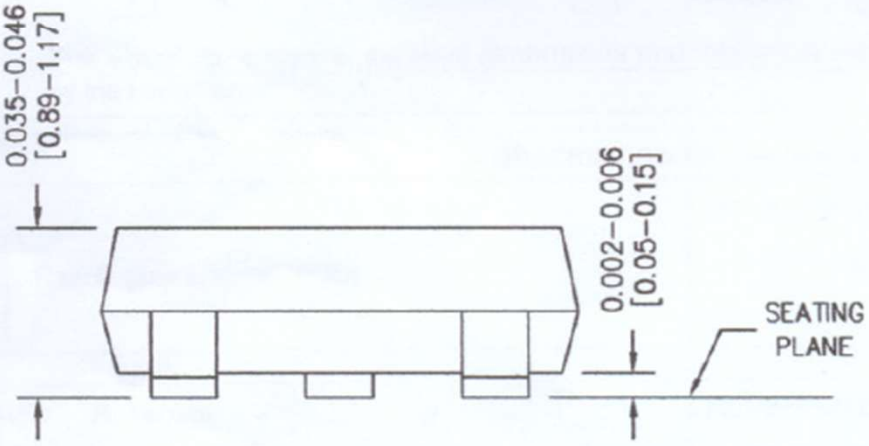

Figure 14: Maximum Forward Biased Safe Operating Area

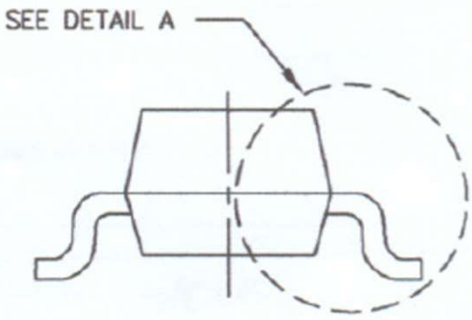
# Package Outline: SOT-23-3L

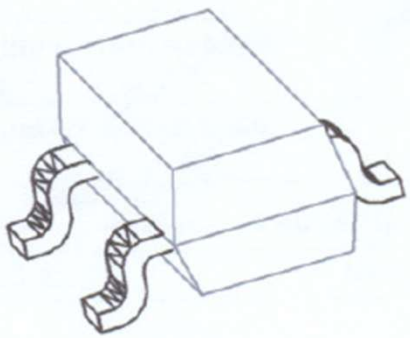



DETAIL A



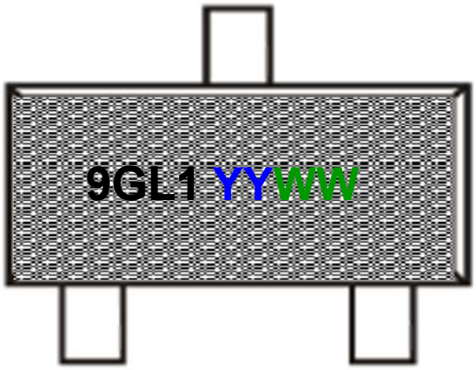



NOTES:
1. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
2. COPLANARITY APPLIES TO THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.004 [0.10].
3. CONTROLLING DIMENSIONS IN MM.

# Marking Information

**YY** = Last two digits of the year

**WW** = Work week




**ICEK900GL10** = ICE is IceMOS logo and
9GL1 is a designated device part number

# Disclaimer