

ICE15N73W N-Channel Enhancement Mode MOSFET

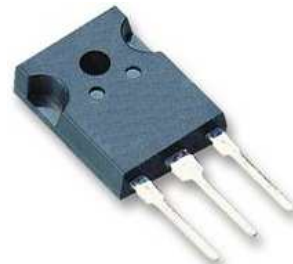
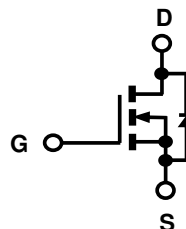
Features

- Low $r_{DS(on)}$
- Ultra Low Gate Charge
- High dv/dt capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems



Lead Free

Product Summary			
I_D	$T_A=25^\circ\text{C}$	15A	Max
$V_{(BR)DSS}$	$I_D=250\mu\text{A}$	730V	Min
$r_{DS(on)}$	$V_{GS}=10\text{V}$	0.18 Ω	Typ
Q_g	$V_{DS}=480\text{V}$	75nC	Typ



TO247
1:G, 2:D,
3:S
(TO-247)

ICEMOS OWNS THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 to 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN & EUROPE.

Maximum ratings at $T_j=25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current ^a	I_D	$T_c=25^\circ\text{C}$ $T_c=100^\circ\text{C}$	15 9	A
Pulsed drain current ^a	$I_{D, \text{pulse}}$	$T_c=25^\circ\text{C}$	35	A
Avalanche energy, single pulse	E_{AS}	$I_D=7.5\text{A}$	280	mJ
Avalanche current, repetitive	I_{AR}	limited by $T_{j\text{max}}$	7.5	A
MOSFET dv/dt ruggedness	dv/dt	$V_{DS}=480\text{V}$, $I_D=15\text{A}$, $T_j=125^\circ\text{C}$	50	V/ns
Gate source voltage	V_{GS}	static	± 20	V
		AC ($f>1\text{Hz}$)	± 30	
Power dissipation	P_{tot}	$T_c=25^\circ\text{C}$	171	W
Operating and storage temperature	T_j, T_{stg}		-55 to +150	$^\circ\text{C}$
Mounting torque ^b		M 3 & 3.5 screws	60	Ncm

^a Limited by $T_{j\text{max}}$

^b When mounted on 1inch square 2oz copper clad FR-4

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

Thermal characteristics

Thermal resistance, junction-case ^b	R_{thJC}		-	-	0.6	°C/W
Thermal resistance, junction-ambient ^b	R_{thJA}	leaded	-	-	62	
Soldering temperature, wave soldering only allowed at leads	T_{sold}	1.6mm (0.063in.) from case for 10 s	-	-	260	°C

Electrical characteristics at $T_j=25^{\circ}\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=250\mu\text{A}$	730	760	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.5	3	3.5	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=730\text{V}$, $V_{GS}=0\text{V}$, $T_j=25^{\circ}\text{C}$	-	0.4	5	μA
		$V_{DS}=730\text{V}$, $V_{GS}=0\text{V}$, $T_j=150^{\circ}\text{C}$	-	135	-	
Gate source leakage current	I_{GSS}	$V_{GS}=\pm 20\text{ V}$, $V_{DS}=0\text{V}$	-	-	100	nA
Drain-source on-state resistance	$r_{DS(on)}$	$V_{GS}=10\text{V}$, $I_D=7.5\text{A}$, $T_j=25^{\circ}\text{C}$	-	0.18	0.25	Ω
		$V_{GS}=10\text{V}$, $I_D=7.5\text{A}$, $T_j=150^{\circ}\text{C}$	-	0.55	-	
Gate resistance	R_G	$f=1\text{ MHz}$, open drain	-	3.0	-	Ω

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=1\text{ MHz}$	-	2816	-	pF
Output capacitance	C_{oss}		-	106	-	
Reverse transfer capacitance	C_{rss}		-	0.4	-	
Transconductance	g_{fs}	$V_{DS}>2*I_D*R_{DS}$, $I_D=7.5\text{A}$	-	14	-	S
Turn-on delay time	$t_{d(on)}$	$V_{DS}=380\text{V}$, $V_{GS}=10\text{V}$, $I_D=15\text{A}$, $R_G=4\Omega$ (External)	-	50	-	ns
Rise time	t_r		-	11	-	
Turn-off delay time	$t_{d(off)}$		-	140	-	
Fall time	t_f		-	6.5	-	

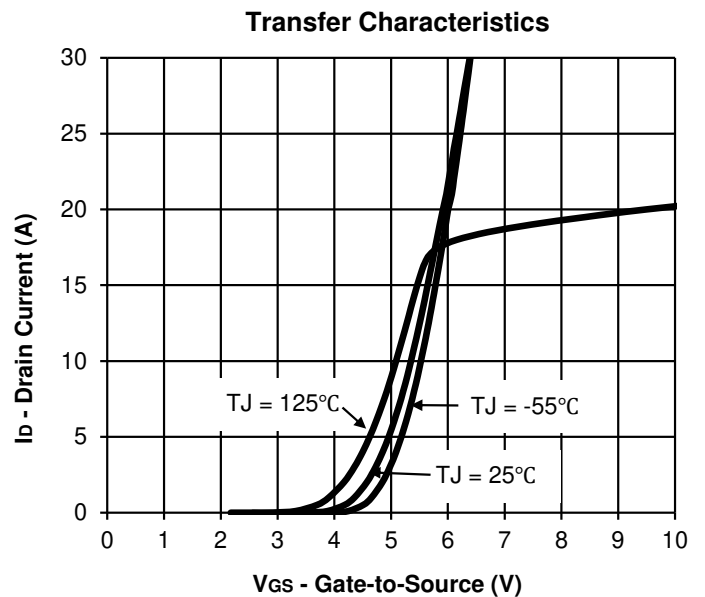
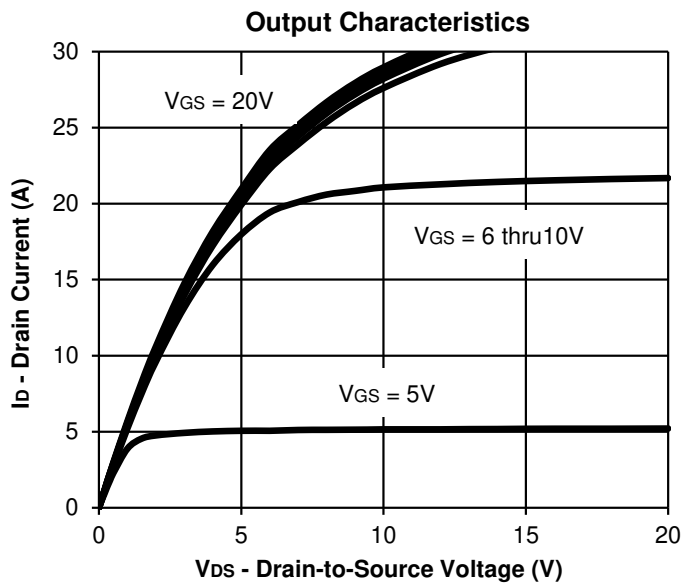
Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

Gate charge characteristics

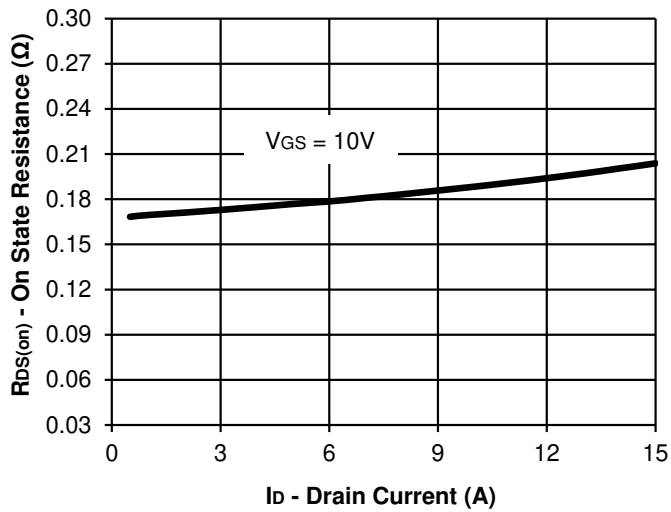
Gate to source charge	Q_{gs}	$V_{DS}=480\text{ V}, I_D=15\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	18	-	nC
Gate to drain charge	Q_{gd}		-	25	-	
Gate charge total	Q_g		-	75	-	
Gate plateau voltage	$V_{plateau}$		-	5.2	-	V

Reverse Diode

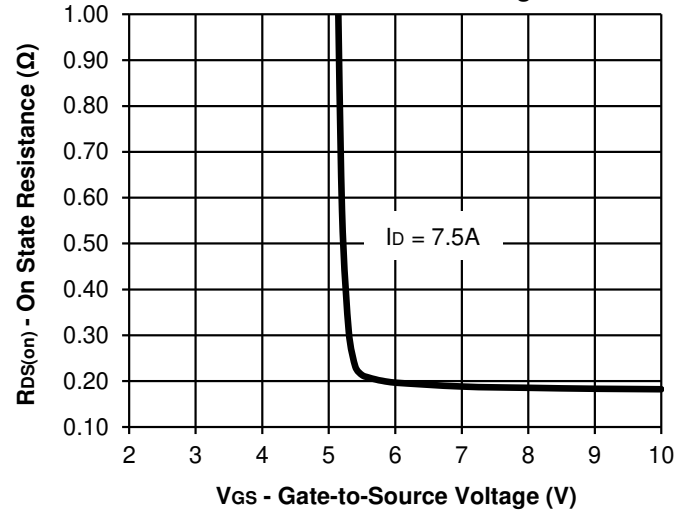
Continuous forward current	I_S	$V_{GS}=0\text{ V}$	-	-	15	A
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_S=I_F$	-	1.0	1.2	V
Reverse recovery time	t_{rr}	$V_{RR}=50\text{ V}, I_S=I_F,$ $d_i I_F/d_t=100\text{ A}/\mu\text{S}$	-	383	-	ns
Reverse recovery charge	Q_{rr}		-	7.0	-	μC
Peak reverse recovery current	I_{rm}		-	37	-	A



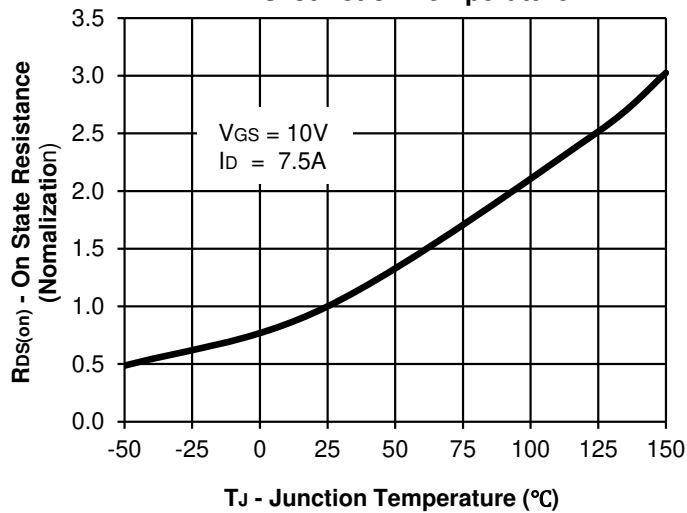
**Drain - Source On-State Resistance
vs. Drain Current**



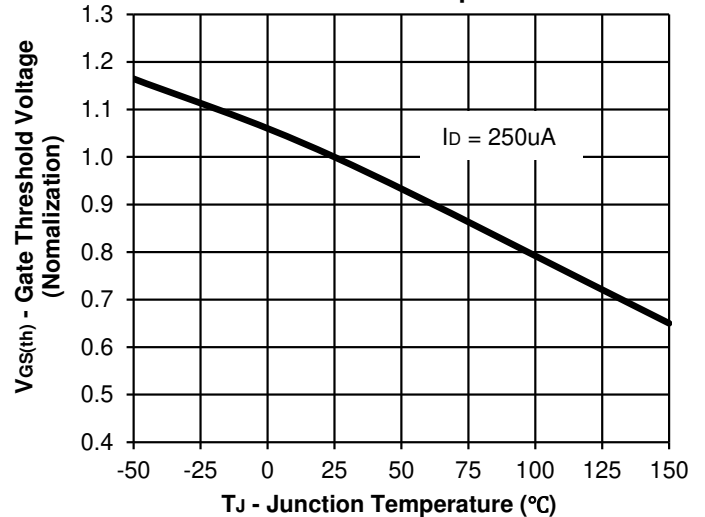
**Drain-Source On-State Resistance
vs. Gate-to-Source Voltage**



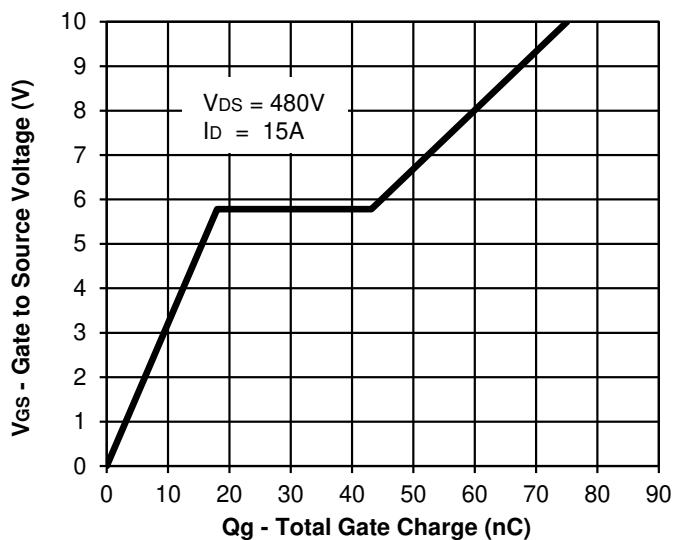
**Drain - Source On State Resistance
vs. Junction Temperature**



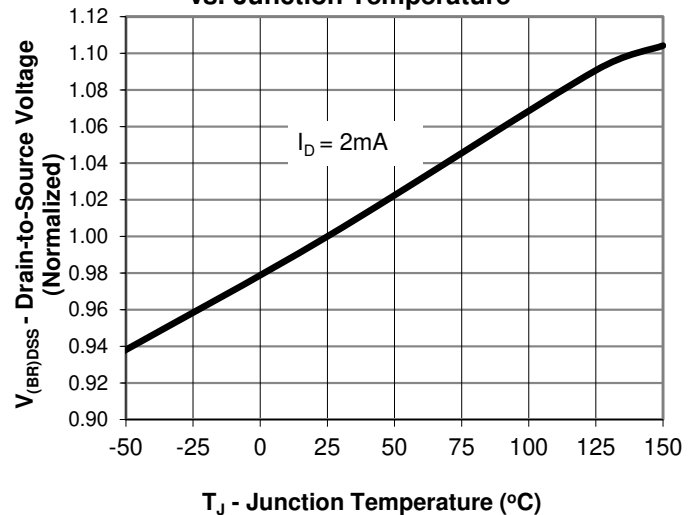
**Gate Threshold Voltage
vs. Junction Temperature**



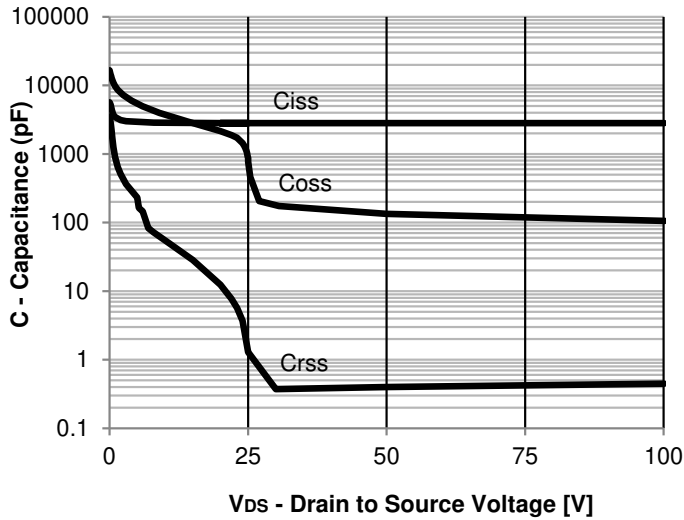
Gate Charge



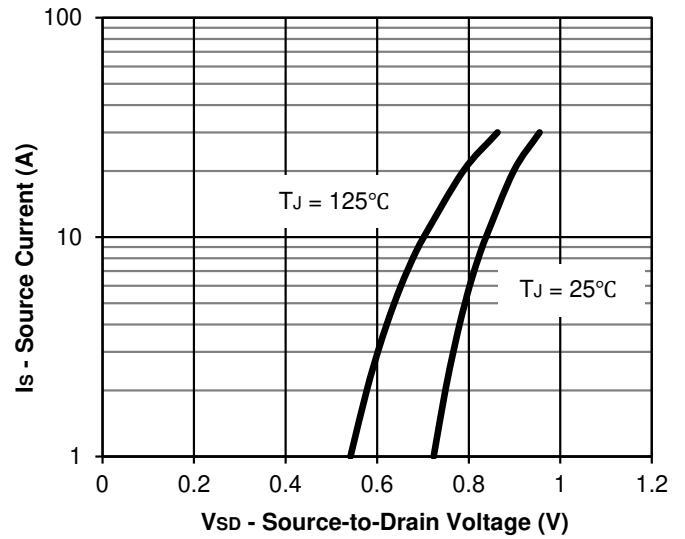
**Drain-to Source Breakdown Voltage
vs. Junction Temperature**



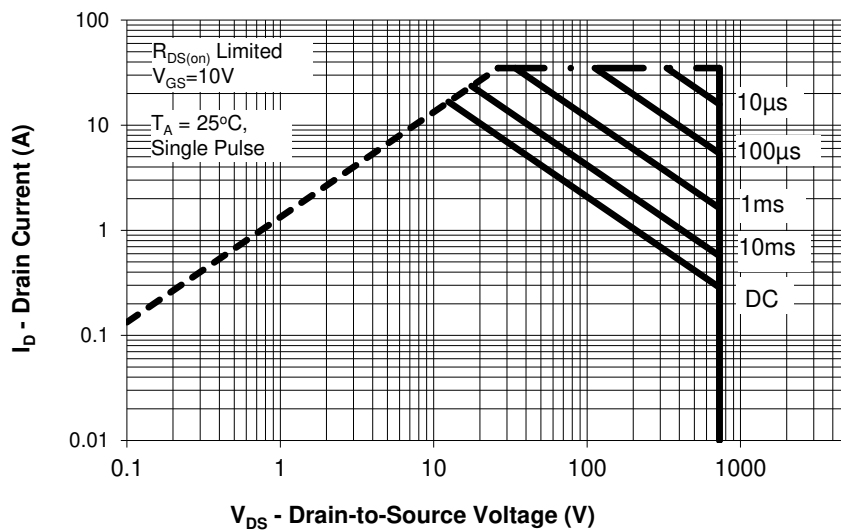
Capacitance



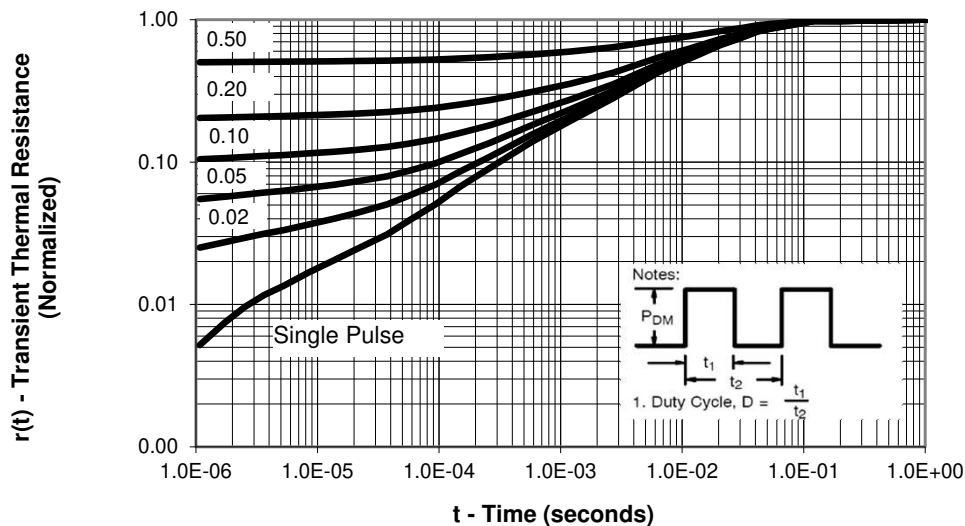
Source-Drain Diode Forward Voltage



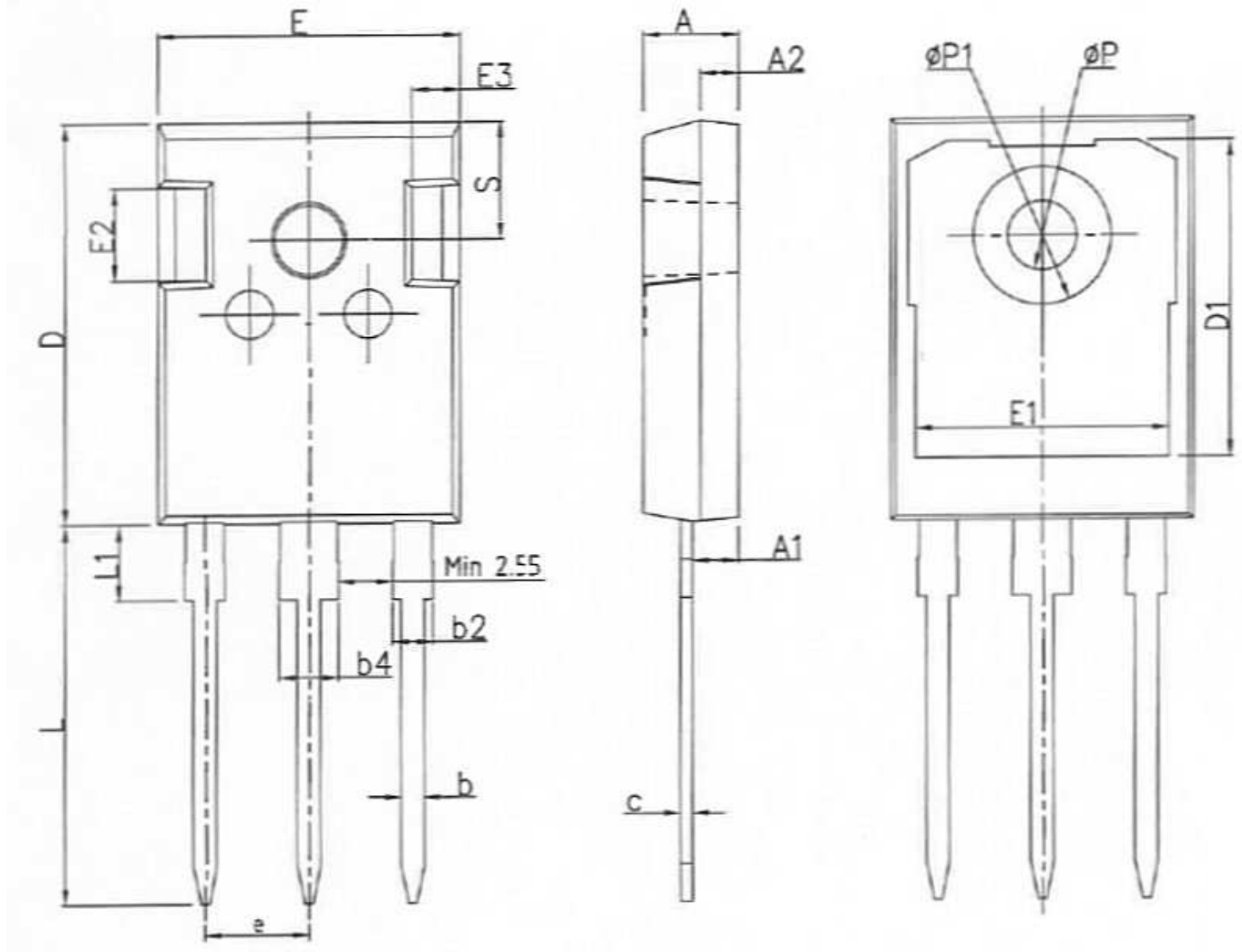
Maximum Rated Forward Biased Safe Operating Area



Transient Thermal Response Junction-to-Ambient



Package Outline: TO-247



Package Outline: TO-247

SYMBOL	unit : mm		
	MIN	NOM	MAX
A	4.8	5	5.2
A1	2.21	2.41	2.59
A2	1.85	2	2.15
b	1.11	1.21	1.36
b	1.91	2.01	2.21
b4	2.91	3.01	3.21
c	0.51	0.61	0.75
D	20.7	21	21.3
D1	16.25	16.55	16.85
E	15.5	15.8	16.1
E1	13	13.3	13.6
E2	4.8	5	5.2
E3	2.3	2.5	2.7
e	5.44BSC		
L	19.62	19.92	20,22
L1	-	-	4.3
ΦP	3.4	3.6	3.8
ΦP1	-	-	7.3
S	6.15BSC		

Marking Information

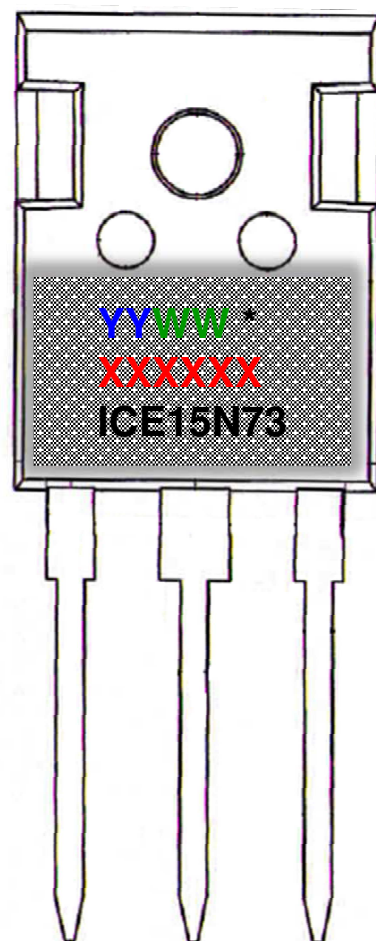
YY = Last two digits of the year

WW = Work week

***** = Site ID

XXXXXX = Lot ID

ICE15N73 = ICE is IceMOS logo and
15N73 is a designated device part
number



Disclaimer

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Revision record

Rev.0 4/24/2023	- new
Rev.1 10/11/2023	- Changed Rdson max spec (@T=25C) from 0.35ohm to 0.25ohm - Changed P_{tot} value (@T=25C) from 208W to 171W - Revised SOA graph due to max Rdson value change
Rev.2 06/20/2025	- Changed the package outline - Changed the number of characters in LOT ID from 5 to 6 on marking information page. - revised the description of patent information on cover page - removed the page of PATENT PORTFOLIO