

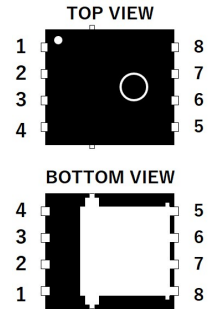
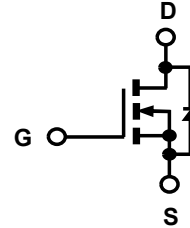
### ICE8S65LK N-Channel Enhancement Mode MOSFET

#### Features

- Low  $r_{DS(on)}$
- Ultra Low Gate Charge
- High  $dv/dt$  capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Optimized design for high performance power systems



Product Summary			
$I_D$	$T_A=25^\circ\text{C}$	8A	Max
$BV_{DSS}$	$I_D=250\mu\text{A}$	650V	Min
$r_{DS(on)}$	$V_{GS}=10\text{V}$	0.33 $\Omega$	Typ
$Q_g$	$V_{DS}=480\text{V}$	12.7nC	Typ



DFN5x6

1-3=Source

4=Gate, 5-8=Drain

ICEMOS AND ITS SISTER COMPANY 3D SEMI OWN THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 to 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN & EUROPE.

**Maximum ratings**<sup>b</sup> at  $T_j=25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$T_c=25^\circ\text{C}$ $T_c=100^\circ\text{C}$	8 5.0	A
Pulsed drain current	$I_{D, pulse}$	$T_c=25^\circ\text{C}$	18	A
Avalanche energy, single pulse	$E_{AS}$	$I_D=2.7\text{A}$	40	mJ
Avalanche current, repetitive	$I_{AR}$	limited by $T_{jmax}$	2.7	A
MOSFET $dv/dt$ ruggedness	$dv/dt$	$V_{DS}=480\text{V}$ , $I_D=8\text{A}$ , $T_j=125^\circ\text{C}$	50.0	V/ns
Gate source voltage	$V_{GS}$	Static	$\pm 20$	V
		AC ( $f>1\text{Hz}$ )	$\pm 30$	
Power dissipation	$P_{tot}$	$T_c=25^\circ\text{C}$	78	W
Operating and storage temperature	$T_j, T_{stg}$		-55 to +150	$^\circ\text{C}$

a When mounted on 1inch square 2oz copper clad FR-4

b limited by  $T_{jmax}$

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

### Thermal characteristics

Thermal resistance, junction-case <sup>a</sup>	$R_{thJC}$		-	-	1.6	°C/W
Thermal resistance, junction-ambient <sup>a</sup>	$R_{thJA}$	leaded	-	-	62	
Soldering temperature, wave soldering only allowed at leads	$T_{sold}$	1.6mm (0.063in.) from case for 10 s	-	-	260	°C

### Electrical characteristics at $T_j=25^{\circ}\text{C}$ , unless otherwise specified

#### Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=250\mu\text{A}$	650	700	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.1	3	3.9	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=650\text{V}, V_{GS}=0\text{V}, T_j=25^{\circ}\text{C}$	-	0.1	1	$\mu\text{A}$
		$V_{DS}=650\text{V}, V_{GS}=0\text{V}, T_j=150^{\circ}\text{C}$	-	100	-	
Gate source leakage current	$I_{GSS}$	$V_{GS}=\pm 20\text{ V}, V_{DS}=0\text{V}$	-	-	100	nA
Drain-source on-state resistance	$r_{DS(on)}$	$V_{GS}=10\text{V}, I_D=4\text{A}, T_j=25^{\circ}\text{C}$	-	0.33	0.40	$\Omega$
		$V_{GS}=10\text{V}, I_D=4\text{A}, T_j=150^{\circ}\text{C}$	-	0.90	-	
Gate resistance	$R_G$	$f=1\text{ MHz}, \text{open drain}$	-	1.2	-	$\Omega$

#### Dynamic characteristics

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, f=1\text{ MHz}$	$V_{DS}=25\text{ V}$	-	674	-	pF
	$C_{oss}$		$V_{DS}=100\text{ V}$	-	30	-	
	$C_{rss}$		$V_{DS}=25\text{ V}$	-	1.54	-	
Transconductance	$g_{fs}$	$V_{DS}>2*I_D*R_{DS}, I_D=4\text{A}$	-	7.1	-	S	
Turn-on delay time	$t_{d(on)}$	$V_{DS}=380\text{V}, V_{GS}=10\text{V}, I_D=8\text{A}, R_G=4\Omega \text{ (External)}$	-	8.6	-	ns	
Rise time	$t_r$		-	6.1	-		
Turn-off delay time	$t_{d(off)}$		-	22.5	-		
Fall time	$t_f$		-	2.7	-		

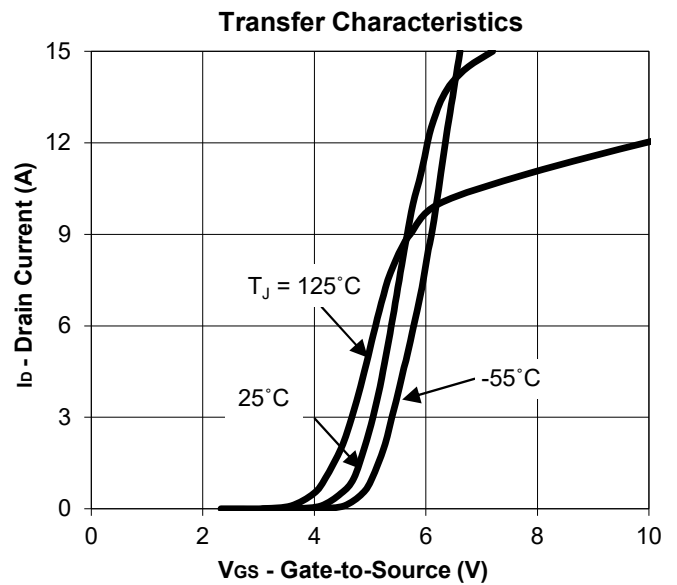
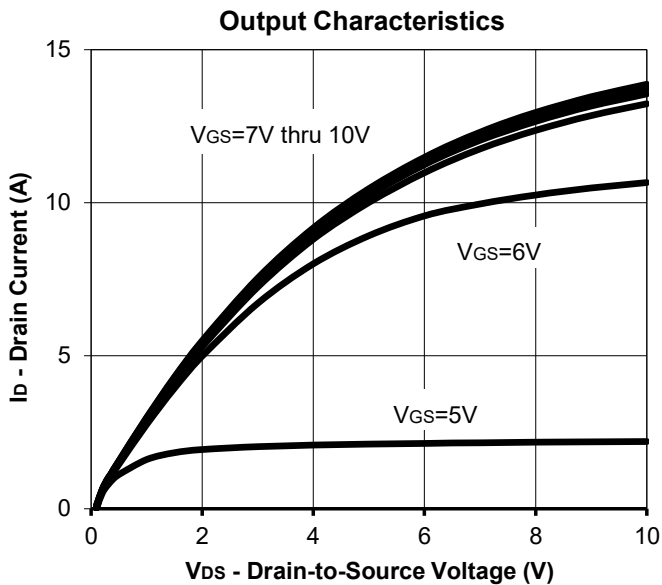
Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

### Gate charge characteristics

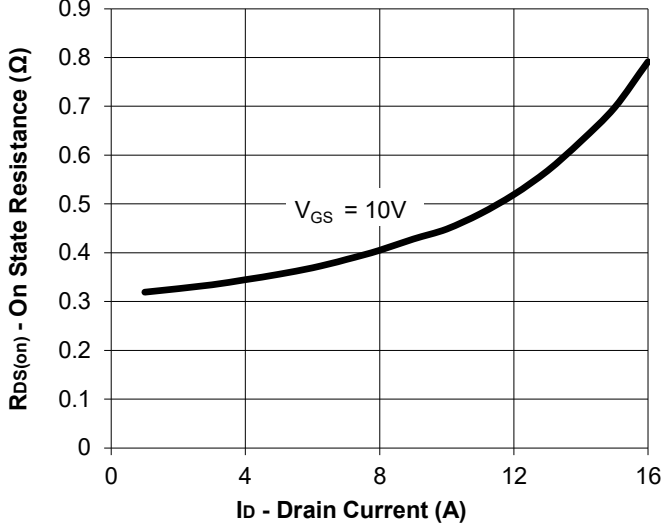
Gate to source charge	$Q_{gs}$	$V_{DS}=480\text{ V}, I_D=8\text{ A},$ $V_{GS}=10\text{ V}$	-	3.8	-	nC
Gate to drain charge	$Q_{gd}$		-	3.6	-	
Gate charge total	$Q_g$		-	12.7	-	
Gate plateau voltage	$V_{plateau}$		-	5.7	-	V

### Reverse Diode

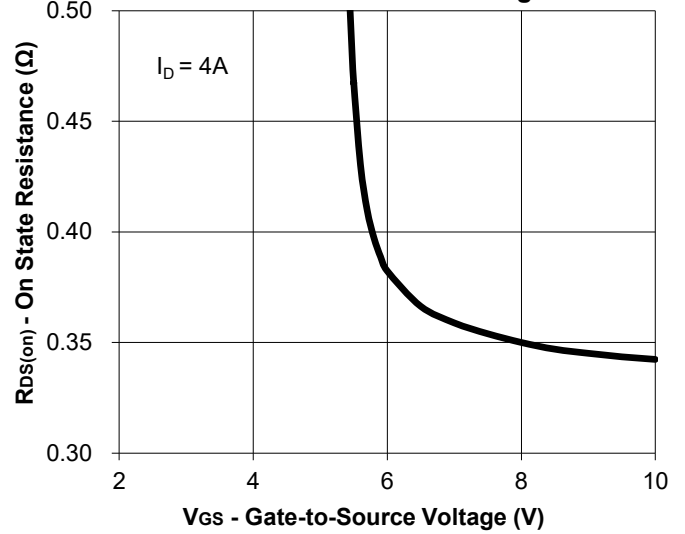
Continuous forward current	$I_S$	$V_{GS}=0\text{ V}$	-	-	8	A
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_S=I_F$	-	0.9	1.2	V
Reverse recovery time	$t_{rr}$	$V_{RR}=50\text{ V}, I_S=I_F,$ $d_{iF}/d_t=100\text{ A}/\mu\text{S}$	-	308	-	ns
Reverse recovery charge	$Q_{rr}$		-	2	-	$\mu\text{C}$
Peak reverse recovery current	$I_{rm}$		-	13	-	A



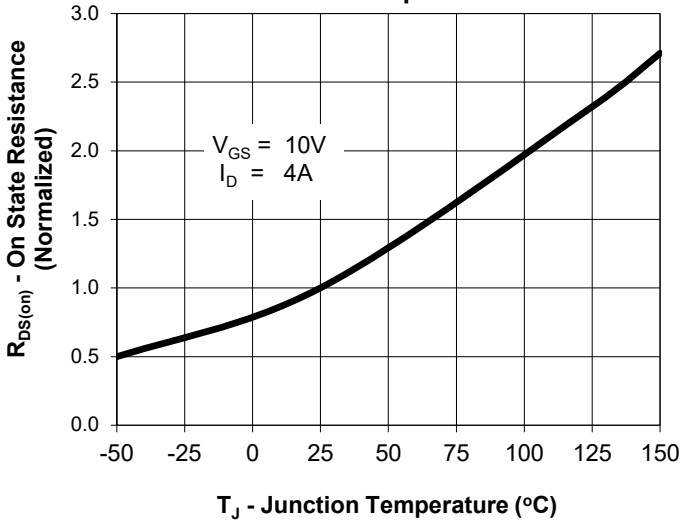
**Drain - Source On-State Resistance vs. Drain Current**



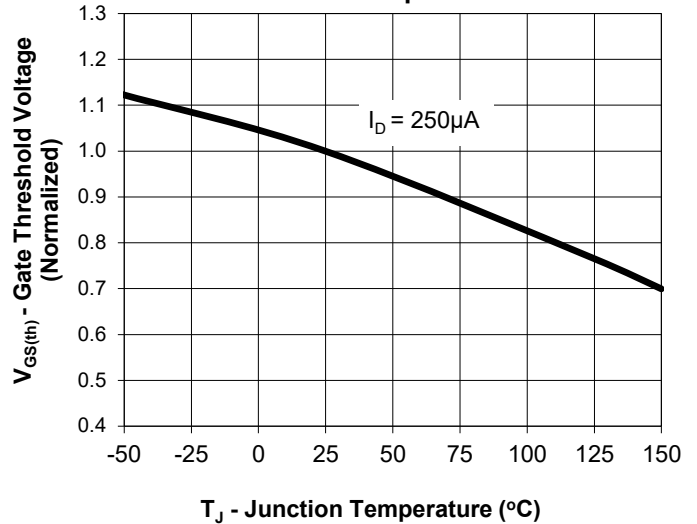
**Drain-Source On-State Resistance vs. Gate-to-Source Voltage**



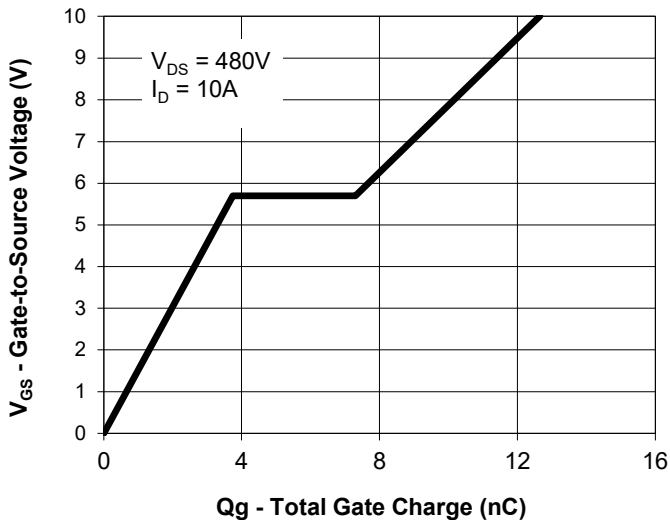
**Drain-Source On State Resistance vs. Junction Temperature**



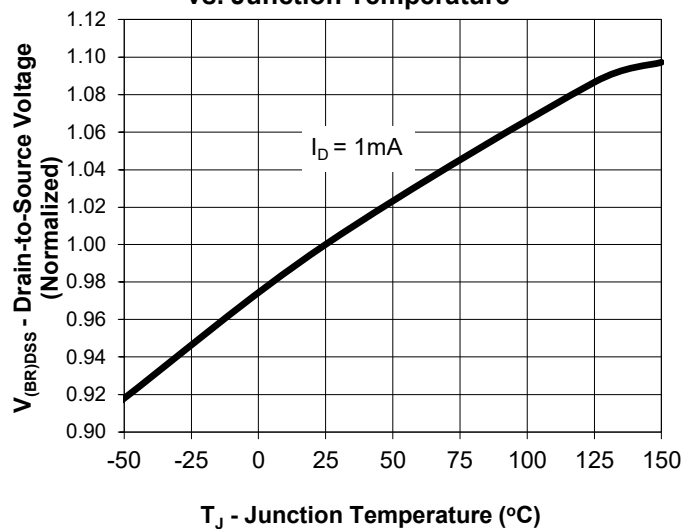
**Gate Threshold Voltage vs. Junction Temperature**



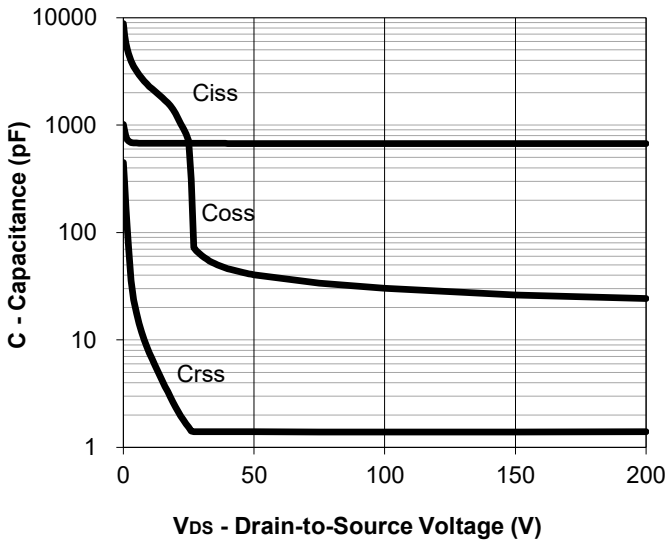
**Gate Charge**



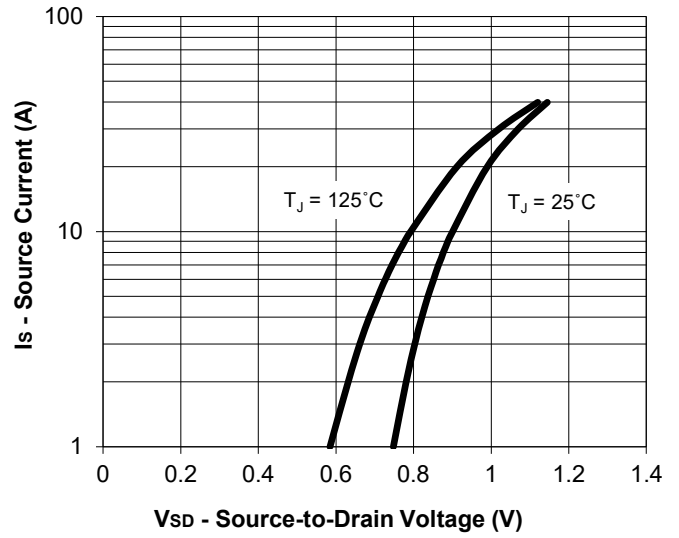
**Drain-to-Source Breakdown Voltage vs. Junction Temperature**



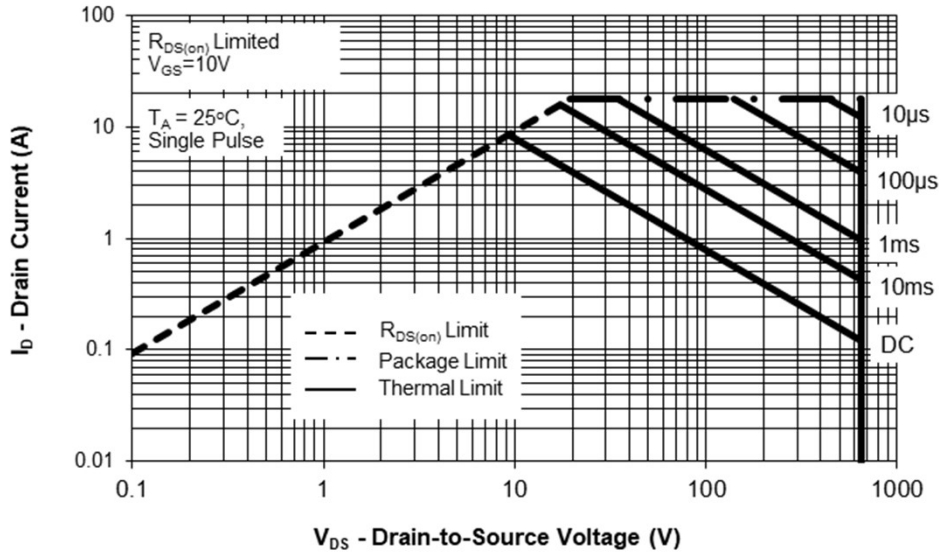
### Capacitance



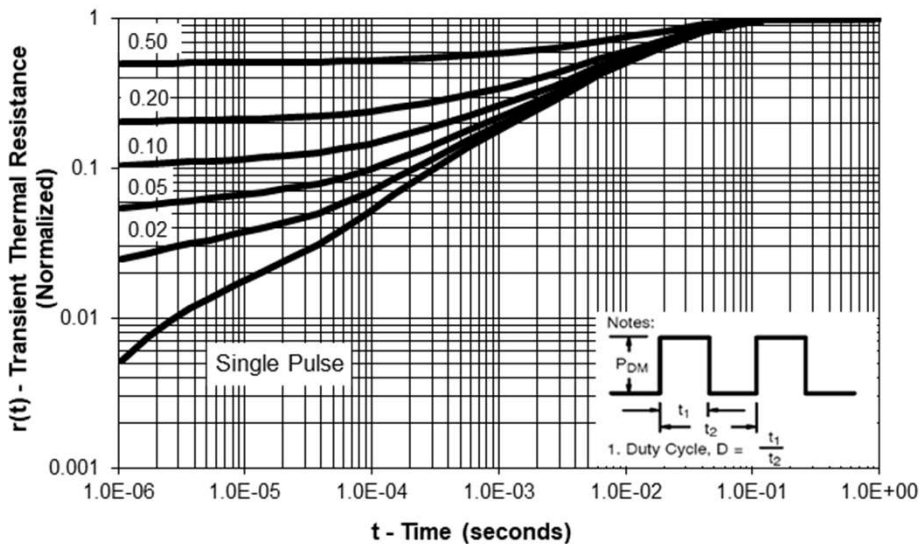
### Source-Drain Diode Forward Voltage



### Maximum Rated Forward Biased Safe Operating Area

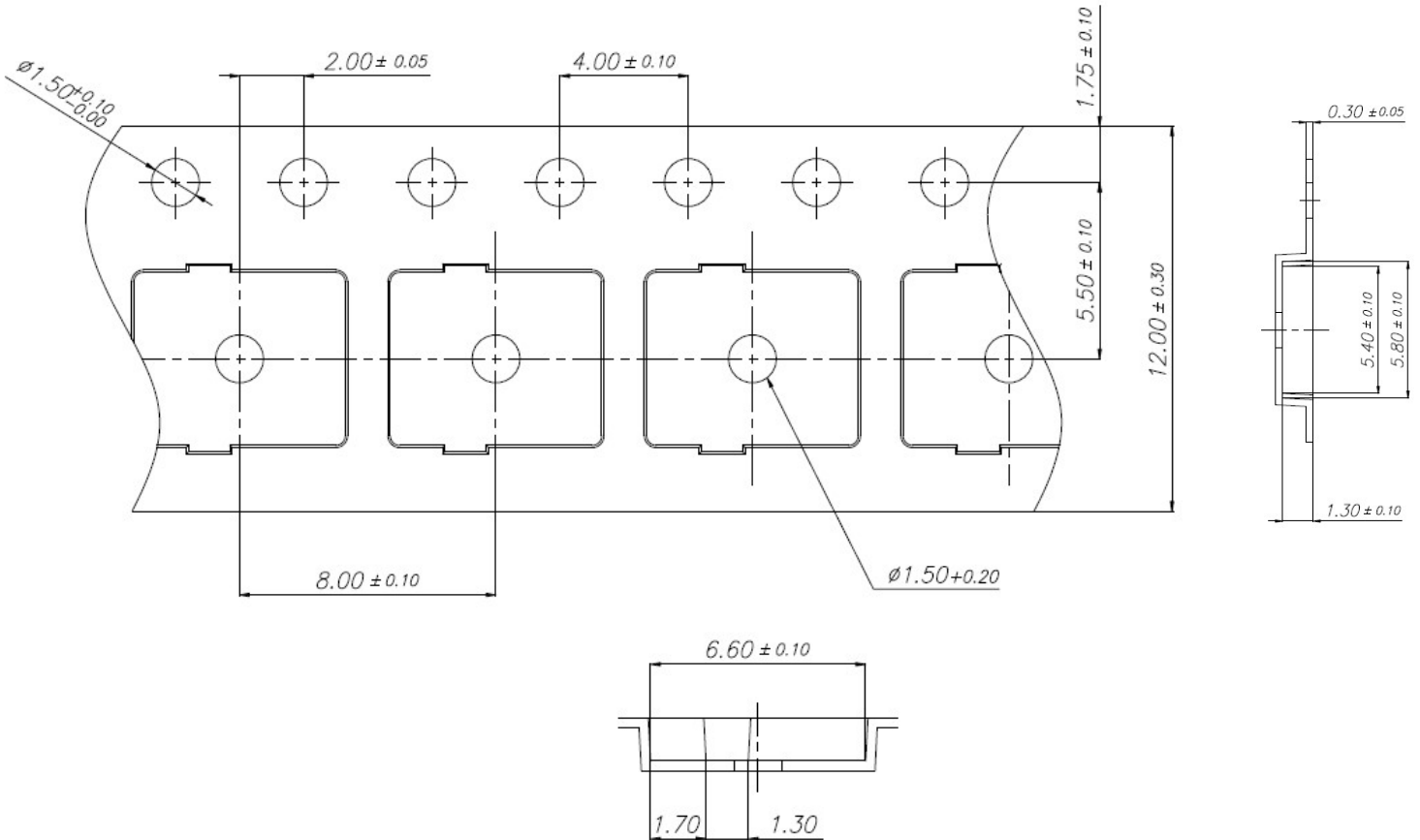


### Transient Thermal Response, Junction-to-Ambient

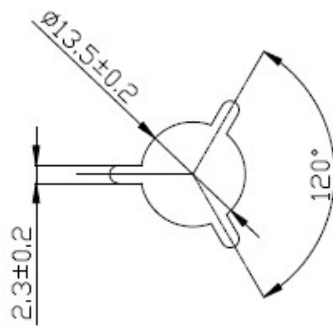
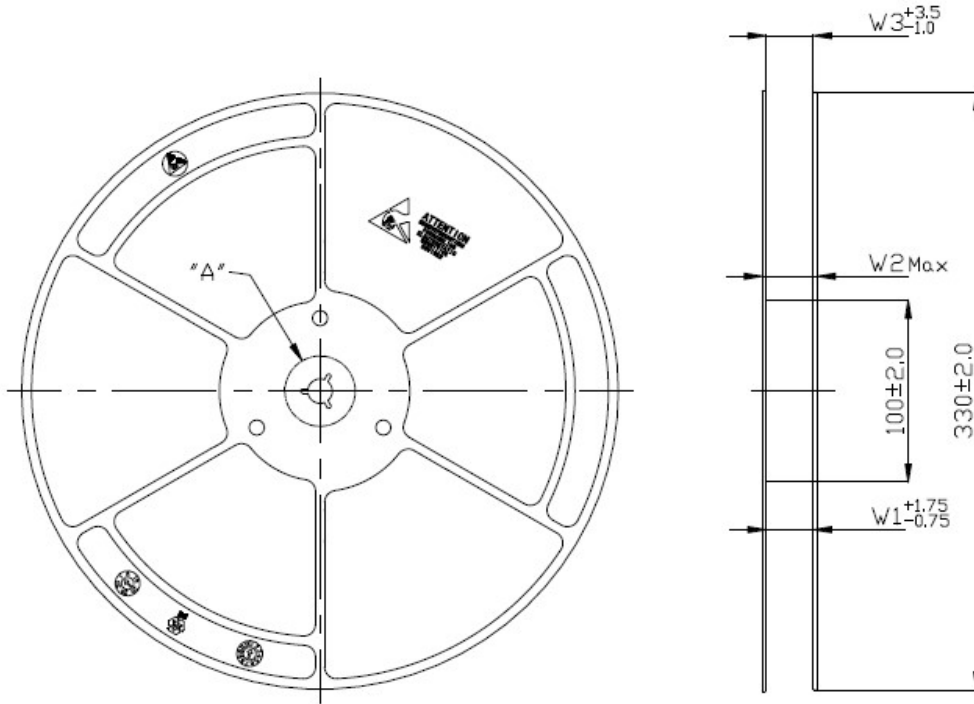




### Tape and Reel Orientation



### Reel and Reel Cap



"A"

W1 = 13.4

W2 = 19.5

W3 = 13.4



## ICEMOS SUPERJUNCTION PATENT PORTFOLIO

### ICEMOS GRANTED PATENTS

US7,429,772

US7,439,178

US7,446,018

US7,579,607

US7,723,172

US7,795,045

US7,846,821

US7,944,018

US8,012,806

US8,030,133

### 3D SEMI PATENTS LICENSED TO ICEMOS

US7,041,560B2

US7,023,069B2

US7,364,994

US7,227,197B2

US7,304,944B2

US7,052,982B2

US7,339,252

US7,410,891

US7,439,583

US7,227,197B2

US6,635,906

US6,936,867

US7,015,104

US9,109,110

US7,271,067

US7,354,818

US7,052,982,

US7,199,006B2

Note: additional patents in China, Korea, Japan, Taiwan, Europe have also been granted to IceMOS and 3D Semi for Superjunction MOSFETs with 70 additional Patent applications in process in the USA and the above listed countries.

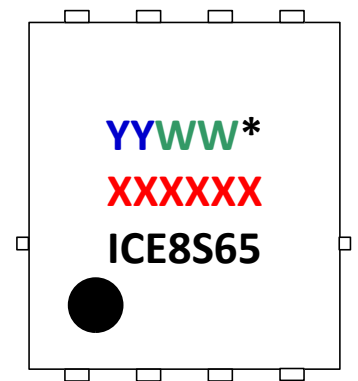
## Marking Information

**YY** = Last two digits of the year

**WW** = Work week

**\*** = Site ID

**XXXXXX** = Lot ID



**ICE8S65** = ICE is IceMOS logo and  
8S65 is a designated device part number

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