IceMOS Technology

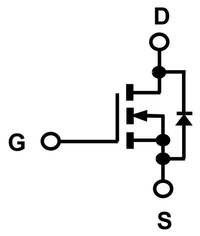
Preliminary Data Sheet
ICE32S60

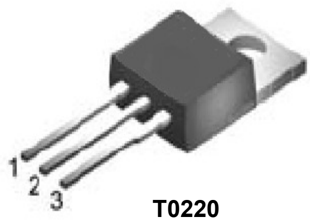
ICE32S60 N-Channel Enhancement Mode MOSFET

Product Summary			
I_D	T_A=25°C	32A	Max
BV_{DSS}	I_D=250uA	600V	Min
$r_{DS(on)}$	V_{GS}=10V	0.07Ω	Typ
Q_g	V_{DS}=480V	47nC	Typ

Features

- Low $r_{DS(on)}$
- Ultra Low Gate Charge
- High d*v*/d*t* capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for hard switching SMPS topologies





T0220

Standard Metal Heatsink

1=Gate, 2=Drain, 3=Source.

RoHS COMPLIANT RoHS (EU) 2015/863

CE

HALOGEN FREE

Lead Free

ICEMOS AND ITS SISTER COMPANY 3D SEMI OWN THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 to 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN & EUROPE.

Maximum ratings [b] at T_j=25°C, unless otherwise specified

Parameter	*Symbol*	*Conditions*	*Value*	*Unit*
Continuous drain current	I_D	T_c=25°C T_c=100°C	32 20.4	A
Pulsed drain current	$I_{D,\ pulse}$	T_c=25°C	102	A
Avalanche energy, single pulse	E_{AS}	I_D=10A	900	mJ
Avalanche current, repetitive	I_{AR}	limited by $T_j$max	10	A
MOSFET d*v*/d*t* ruggedness	d*v*/d*t*	V_{DS}=480V, I_D=32A, T_j=125°C	50.0	V/ns
Gate source voltage	V_{GS}	Static	±20	V
		AC (*f*>1Hz)	±30	
Power dissipation	P_{tot}	T_c=25°C	231	W
Operating and storage temperature	T_j, T_{stg}		-55 to +150	°C
Mounting torque [a]		M 3 & 3.5 screws	60	Ncm

a When mounted on 1inch square 2oz copper clad FR-4
b limited by T_{jmax}
* Preliminary Data Sheet – Specifications subject to change

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

Thermal characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Thermal resistance, junction-case [a]	R_{thJC}		-	-	0.54	°C/W
Thermal resistance, junction-ambient [a]	R_{thJA}	leaded	-	-	62	
Soldering temperature, wave soldering only allowed at leads	T_{sold}	1.6mm (0.063in.) from case for 10 s	-	-	260	°C

Electrical characteristics [b] at T_j=25°C, unless otherwise specified

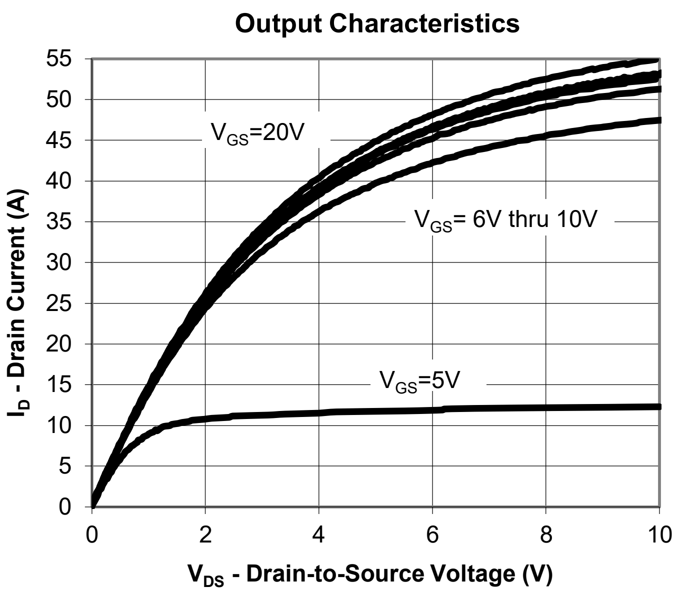
Static characteristics

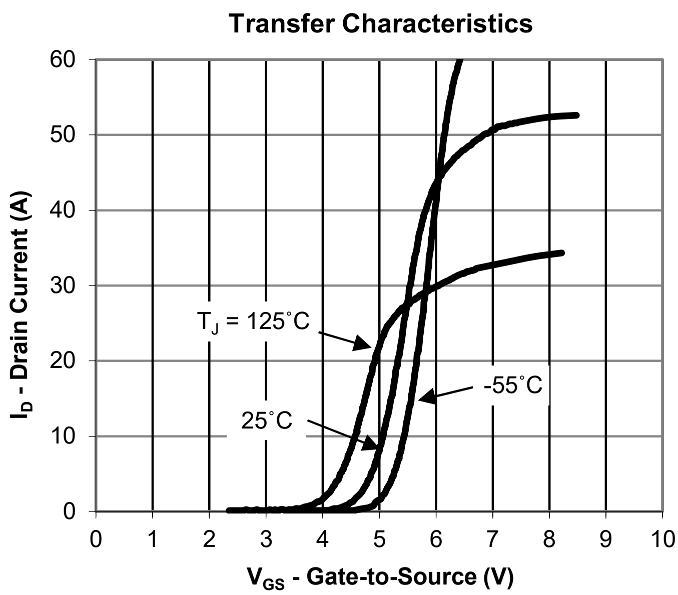
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=250µA	600	640	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250µA	2.5	3	3.5	
Zero gate voltage drain current	I_{DSS}	V_{DS}=600V, V_{GS}=0V, T_j=25°C	-	1	5	µA
		V_{DS}=600V, V_{GS}=0V, T_j=150°C	-	100	-	
Gate source leakage current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0V	-	-	100	nA
Drain-source on-state resistance	$r_{DS(on)}$	V_{GS}=10V, I_D=16A, T_j=25°C	-	0.07	0.078	Ω
		V_{GS}=10V, I_D=16A, T_j=150°C	-	0.2	-	
Gate resistance	R_G	f=1 MHZ, open drain	-	1.1	-	Ω

Dynamic characteristics

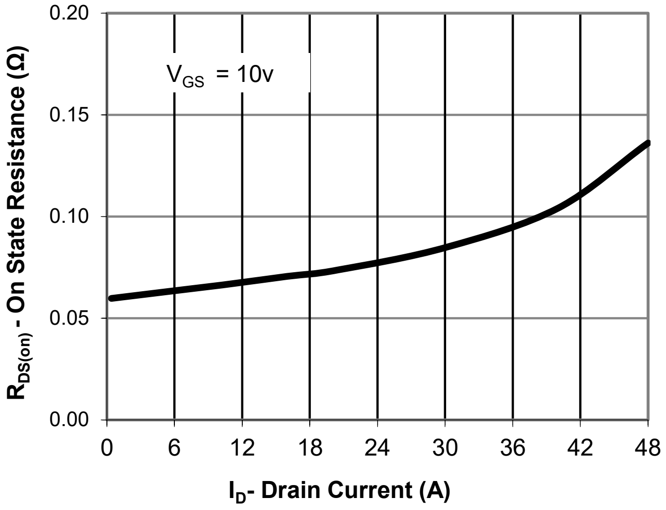
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=25V, f=1 MHz	-	2340	-	pF
Output capacitance	C_{oss}		-	300	-	
Reverse transfer capacitance	C_{rss}		-	4	-	
Output capacitance	C_{oss}	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz	-	103	-	
Transconductance	g_{fs}	V_{DS}>2*I_D*R_{DS}, I_D=16A	-	30	-	S
Turn-on delay time	$t_{d(on)}$	V_{DS}=380V, V_{GS}=10V, I_D=32A, R_G=4Ω (External)	-	28	-	ns
Rise time	t_r		-	9	-	
Turn-off delay time	$t_{d(off)}$		-	66	-	
Fall time	t_f		-	3	-	

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Gate charge characteristics						
Gate to source charge	Q_{gs}	V_{DS}=480 V, I_D=32A, V_{GS}=10 V	-	10	-	nC
Gate to drain charge	Q_{gd}		-	8.5	-	
Gate charge total	Q_g		-	47	-	
Gate plateau voltage	$V_{plateau}$		-	5.5	-	V
Reverse Diode						
Continuous forward current	I_S	V_{GS}=0V	-	-	32	A
Diode forward voltage	V_{SD}	V_{GS}=0V, I_S=I_F	-	1.0	1.2	V
Reverse recovery time	t_{rr}	V_{RR}=50V, I_S=I_F, d_{iF}/d_t=100 A/µS	-	400	-	ns
Reverse recovery charge	Q_{rr}		-	6.8	-	µC
Peak reverse recovery current	I_{rm}		-	40	-	A

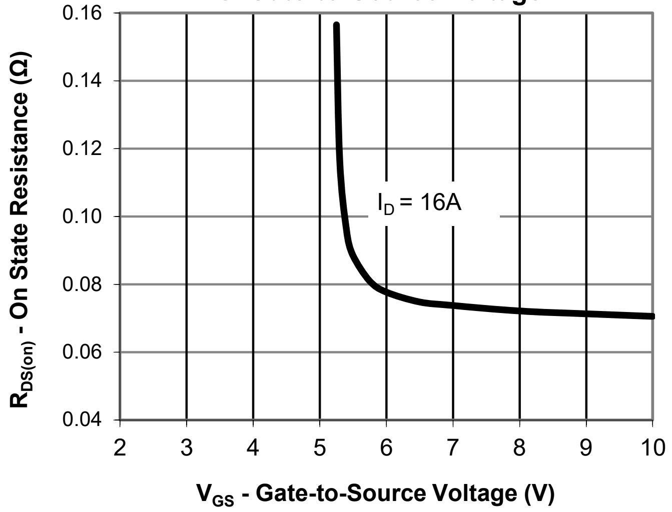




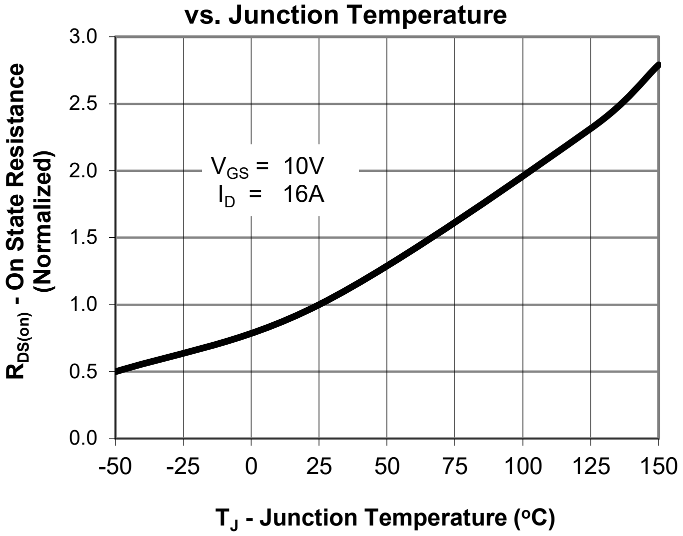
Drain-Source On-State Resistance vs. Drain Current



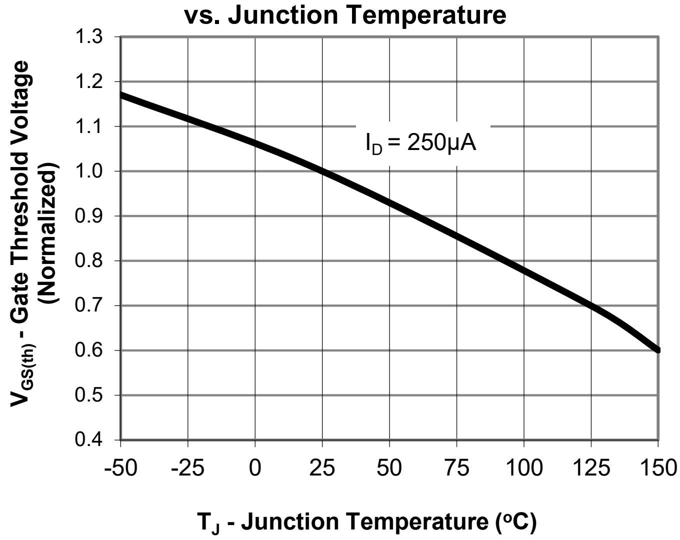
Drain-Source On-State Resistance vs. Gate-to-Source Voltage



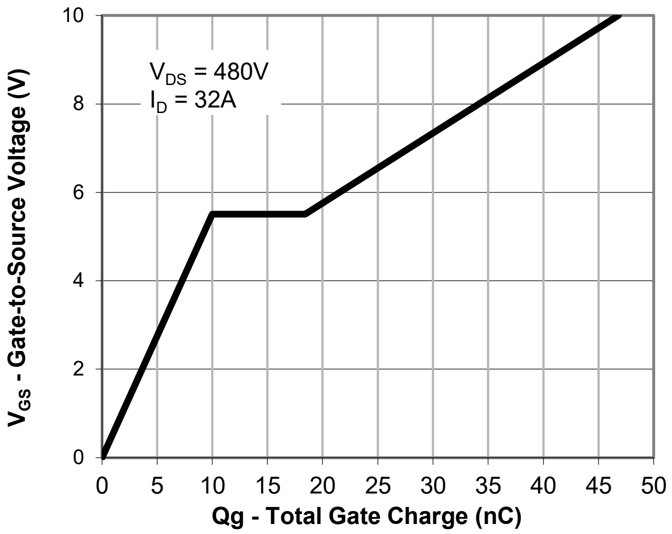
Drian-Source On State Resistance vs. Junction Temperature



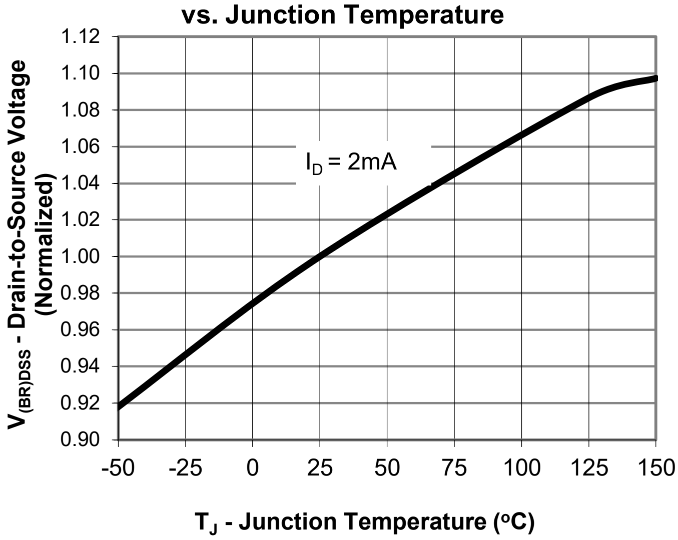
Gate Threshold Voltage vs. Junction Temperature



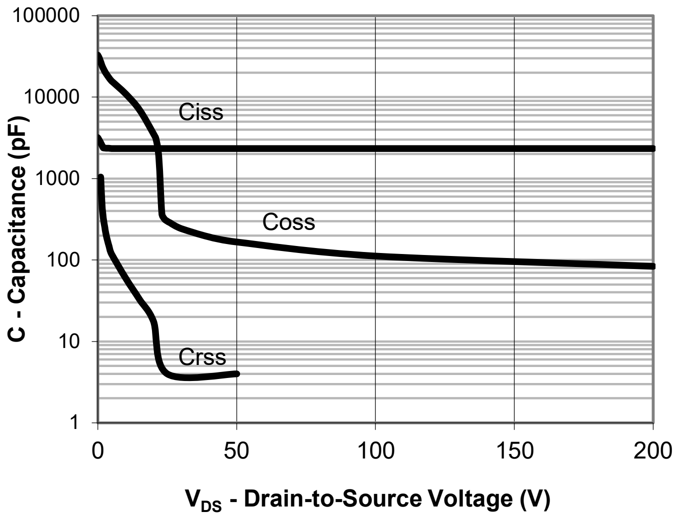
Gate Charge



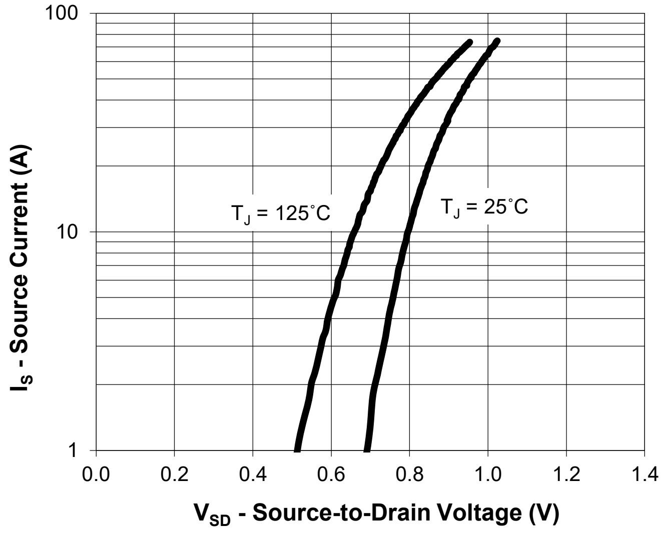
Drain-toSource Breakdown Voltage vs. Junction Temperature



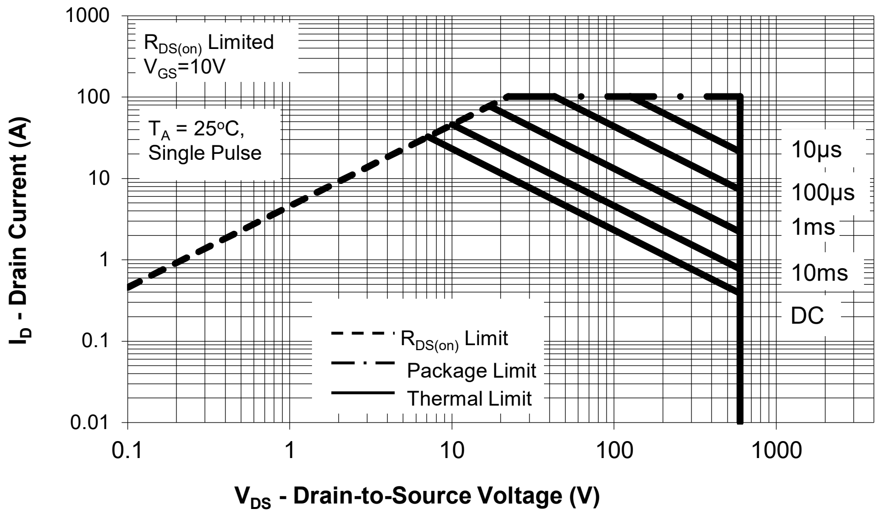
Capacitance



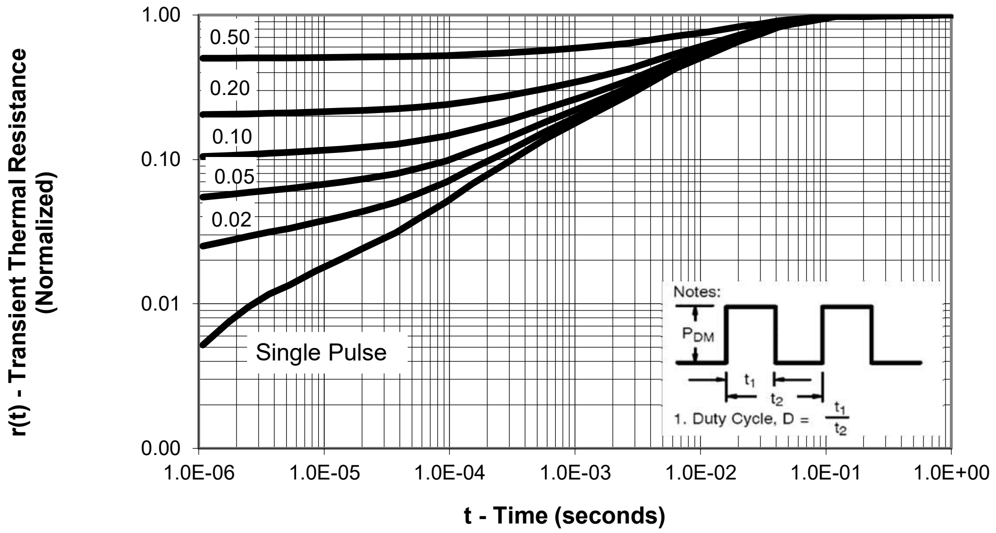
Source-Drain Diode Forward Voltage



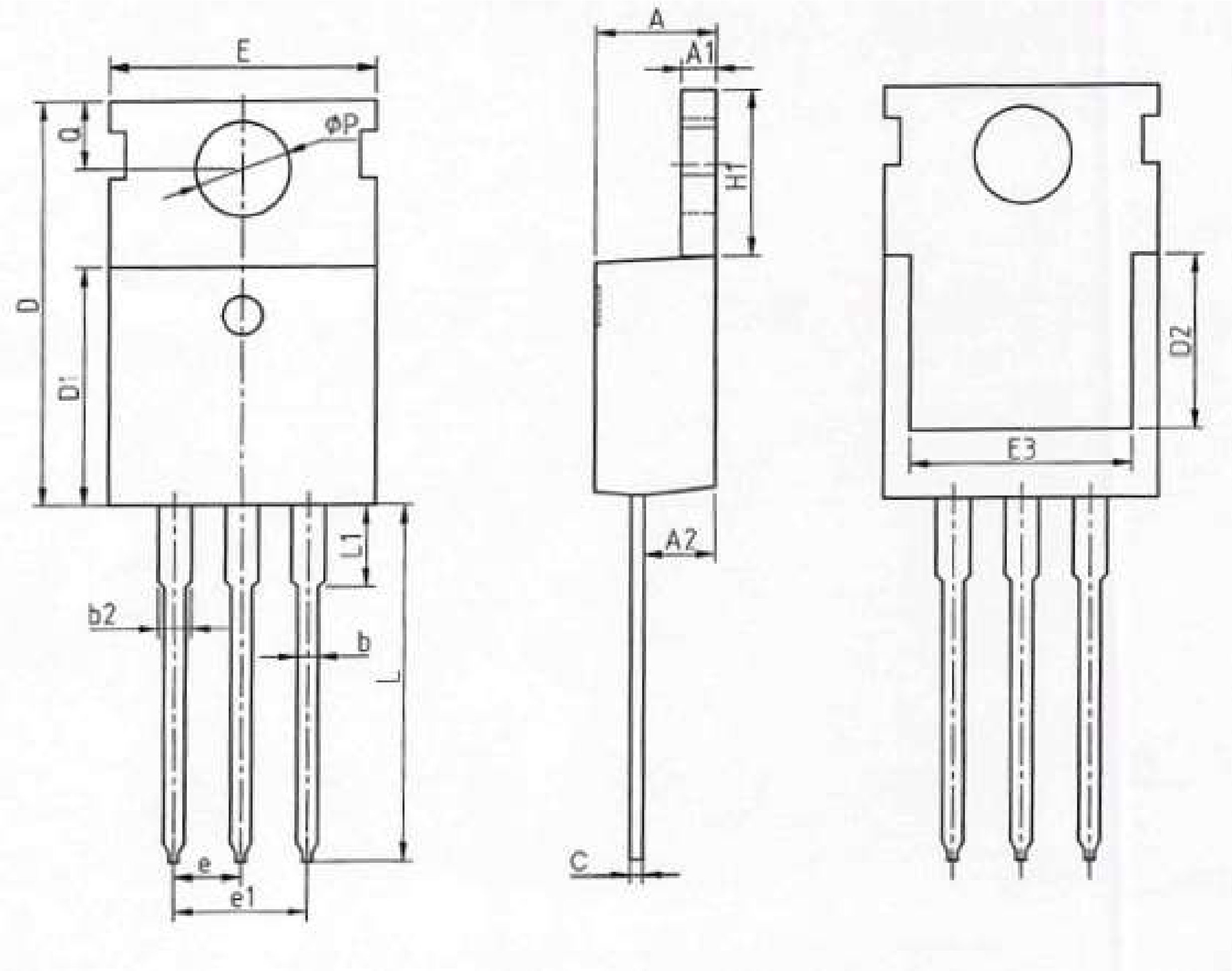
Maximum Rated Forward Biased Safe Operating Area



Transient Thermal Response, Junction-to-Ambient



Package Outline: TO-220



Package Outline: TO-220

COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX
A	4.37	4.57	4.70
A1	1.25	1.30	1.40
A2	2.20	2.40	2.60
b	0.70	0.80	0.95
b2	1.17	1.27	1.47
c	0.45	0.50	0.60
D	15.10	15.60	16.10
D1	8.80	9.10	9.40
D2	5.50	-	-
E	9.70	10.00	10.30
E3	7.00	-	-
e	2.54 BSC		
e1	5.08 BSC		
H1	6.25	6.50	6.85
L	12.75	13.50	13.80
L1	-	3.10	3.40
ΦP	3.40	3.60	3.80
Q	2.60	2.80	3.00

ICEMOS SUPERJUNCTION PATENT PORTFOLIO

ICEMOS GRANTED PATENTS

US7,429,772
US7,439,178
US7,446,018
US7,579,607
US7,723,172
US7,795,045
US7,846,821
US7,944,018
US8,012,806
US8,030,133

3D SEMI PATENTS LICENSED TO ICEMOS

US7,041,560B2
US7,023,069B2
US7,364,994
US7,227,197B2
US7,304,944B2
US7,052,982B2
US7,339,252
US7,410,891
US7,439,583
US7,227,197B2
US6,635,906
US6,936,867
US7,015,104
US9,109,110
US7,271,067
US7,354,818
US7,052,982,
US7,199,006B2

Note: additional patents in China, Korea, Japan, Taiwan, Europe have also been granted to IceMOS and 3D Semi for Superjunction MOSFETs with 70 additional Patent applications in process in the USA and the above listed countries.

Marking Information

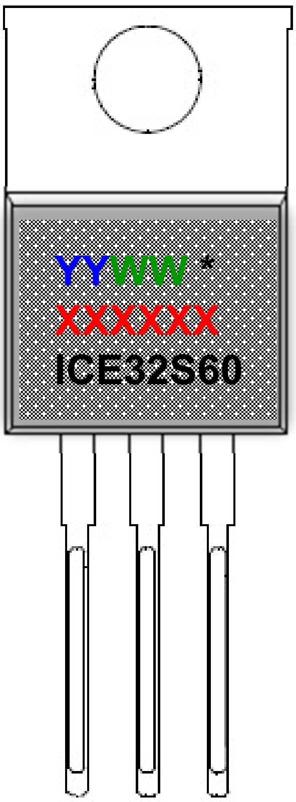
YY = Last two digits of the year

WW = Work week calendar on Icemos subcon assembly & test house

* = Site ID

XXXXXX = Lot ID

ICE32S60 = ICE is IceMOS logo and 32S60 is a designated device part number



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