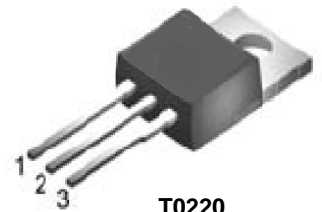
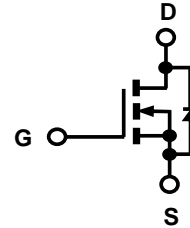


## ICE22N60 N-Channel Enhancement Mode MOSFET

### Features

- Low  $r_{DS(on)}$
- Ultra Low Gate Charge
- High  $dv/dt$  capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems

Product Summary			
$I_D$	$T_c=25^\circ\text{C}$	22A	Max
$V_{(BR)DSS}$	$I_D=250\mu\text{A}$	600V	Min
$r_{DS(on)}$	$V_{GS}=10\text{V}$	0.14 $\Omega$	Typ
$Q_g$	$V_{DS}=480\text{V}$	72nC	Typ



TO220

Standard Metal Heatsink

1=Gate, 2=Drain, 3=Source.



ICEMOS AND ITS SISTER COMPANY 3D SEMI OWN THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 to 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN & EUROPE.

**Maximum ratings**<sup>b</sup> at  $T_j=25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current <sup>a</sup>	$I_D$	$T_c=25^\circ\text{C}$	22	A
		$T_c=100^\circ\text{C}$	13	
Pulsed drain current	$I_{D,pulse}$	$T_c=25^\circ\text{C}$	82	A
Avalanche energy, single pulse	$E_{AS}$	$I_D=11\text{A}$	690	mJ
Avalanche current, repetitive	$I_{AR}$	limited by $T_j,max$	11	A
MOSFET $dv/dt$ ruggedness	$dv/dt$	$V_{DS}=480\text{V}$ , $I_D=22\text{A}$ , $T_j=125^\circ\text{C}$	50.0	V/ns
Gate source voltage	$V_{GS}$	Static	$\pm 20$	V
		AC ( $f>1\text{Hz}$ )	$\pm 30$	
Power dissipation	$P_{tot}$	$T_c=25^\circ\text{C}$	208	W
Operating and storage temperature	$T_j, T_{stg}$		-55 to +150	$^\circ\text{C}$

<sup>a</sup> When mounted on 1inch square 2oz copper clad FR-4

<sup>b</sup> Pulse width limited by  $T_{j,max}$

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

### Thermal characteristics

Thermal resistance, junction-case <sup>a</sup>	$R_{thJC}$		-	-	0.6	°C/W
Thermal resistance, junction-ambient <sup>a</sup>	$R_{thJA}$	leaded	-	-	62	
Soldering temperature, wave soldering only allowed at leads	$T_{sold}$	1.6mm (0.063in.) from case for 10 s	-	-	260	°C

### Electrical characteristics , at $T_j=25^{\circ}\text{C}$ , unless otherwise specified

#### Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=250\mu\text{A}$	600	640	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.1	3	3.9	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=600\text{V}, V_{GS}=0\text{V}, T_j=25^{\circ}\text{C}$	-	0.9	1	$\mu\text{A}$
		$V_{DS}=600\text{V}, V_{GS}=0\text{V}, T_j=150^{\circ}\text{C}$	-	100	-	
Gate source leakage current	$I_{GSS}$	$V_{GS}=\pm 20\text{ V}, V_{DS}=0\text{V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=11\text{A}, T_j=25^{\circ}\text{C}$	-	0.14	0.16	$\Omega$
		$V_{GS}=10\text{V}, I_D=11\text{A}, T_j=150^{\circ}\text{C}$	-	0.40	-	
Gate resistance	$R_G$	$f=1\text{ MHz}, \text{open drain}$	-	3.5	-	$\Omega$

#### Dynamic characteristics

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V}, f=1\text{ MHz}$	-	2730	-	$\mu\text{F}$
Reverse transfer capacitance	$C_{rss}$		-	5	-	
Output capacitance	$C_{oss}$	$V_{GS}=0\text{ V}, V_{DS}=100\text{ V}, f=1\text{ MHz}$	-	97	-	
Transconductance	$g_{fs}$	$V_{DS}>2 \cdot I_D \cdot R_{DS}, I_D=11\text{A}$	-	23	-	S
Turn-on delay time	$t_{d(on)}$	$V_{DS}=380\text{V}, V_{GS}=10\text{V}, I_D=11\text{A}, R_G=4\Omega \text{ (External)}$	-	27.4	-	ns
Rise time	$t_r$		-	11.6	-	
Turn-off delay time	$t_{d(off)}$		-	110	-	
Fall time	$t_f$		-	3.5	-	

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

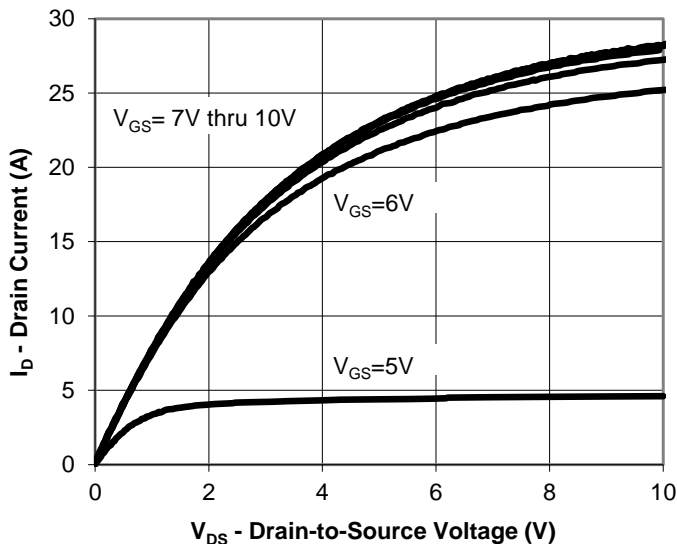
### Gate charge characteristics

Gate to source charge	$Q_{gs}$	$V_{DS}=480\text{ V}, I_D=22\text{ A},$ $V_{GS}=10\text{ V}$	-	15.8	-	nC
Gate to drain charge	$Q_{gd}$		-	27.9	-	
Gate charge total	$Q_g$		-	72	-	
Gate plateau voltage	$V_{plateau}$		-	4.8	-	V

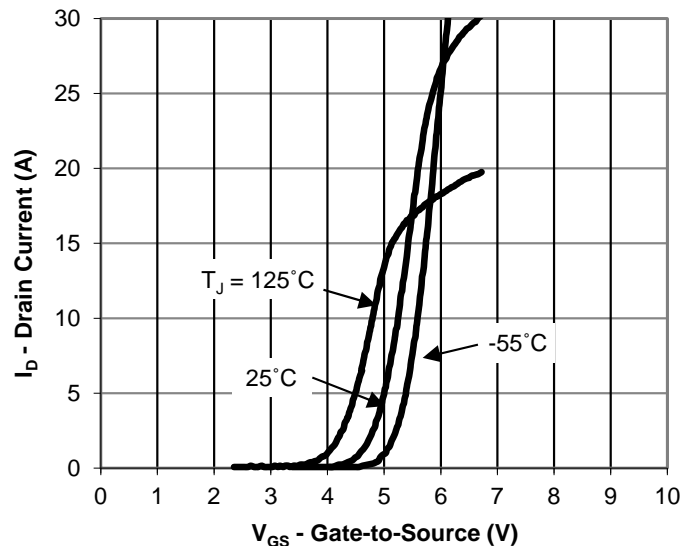
### Reverse Diode

Continuous forward current	$I_{SD}$	$V_{GS}=0\text{ V}$	-	-	22	A
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_S=I_F$	-	1.0	1.2	V
Reverse recovery time	$t_{rr}$	$V_{RR}=50\text{ V}, I_S=I_F,$ $d_iF/d_t=100\text{ A}/\mu\text{S}$	-	440	-	ns
Reverse recovery charge	$Q_{rr}$		-	8	-	$\mu\text{C}$
Peak reverse recovery current	$I_{rm}$		-	35	-	A

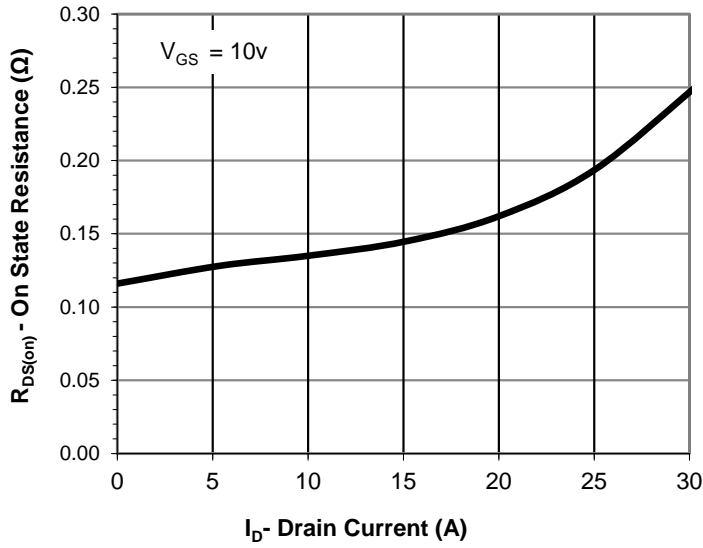
#### Output Characteristics



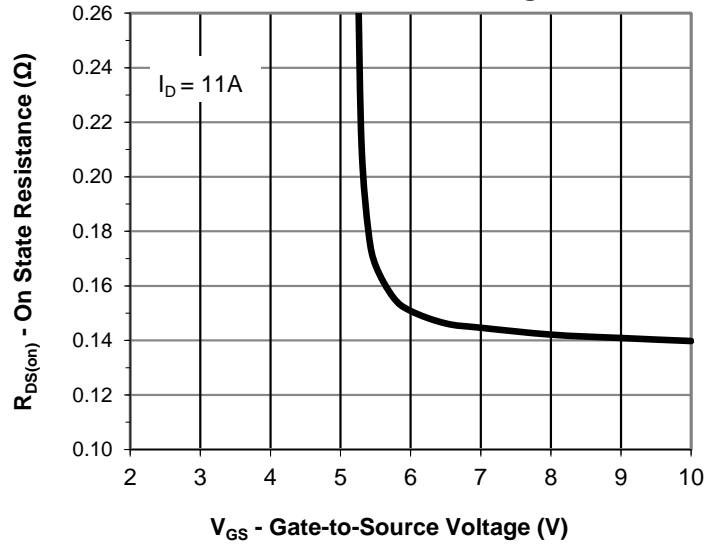
#### Transfer Characteristics



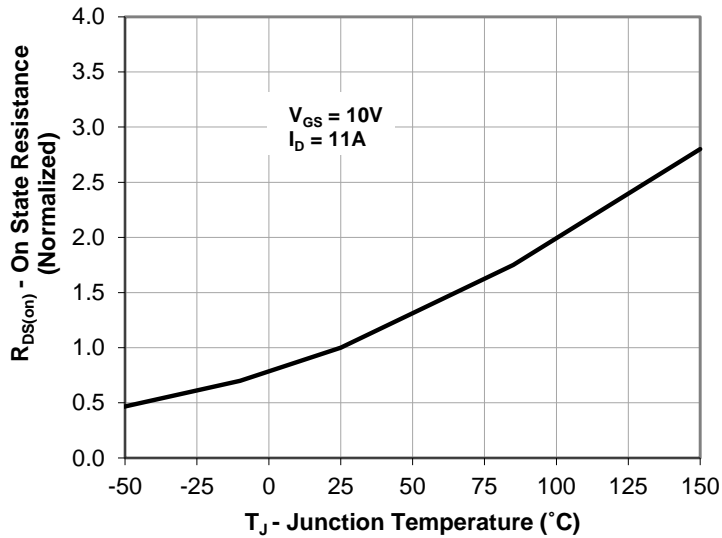
**Drain-Source On-State Resistance vs. Drain Current**



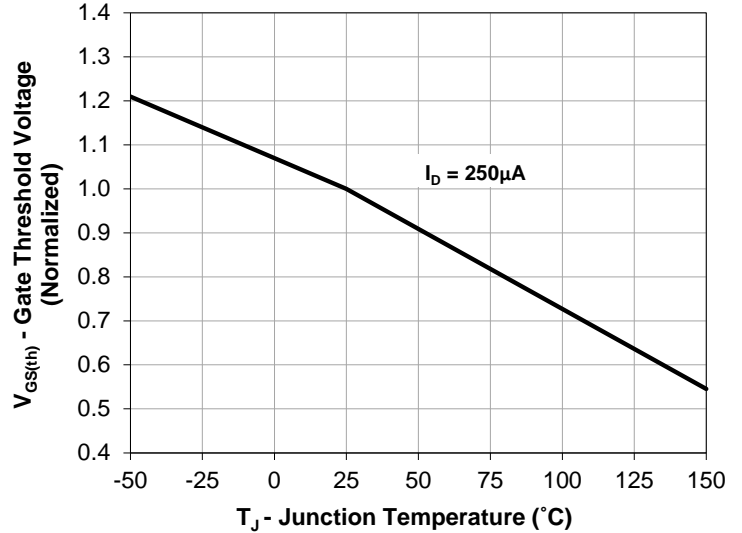
**Drain-Source On-State Resistance vs. Gate-to-Source Voltage**



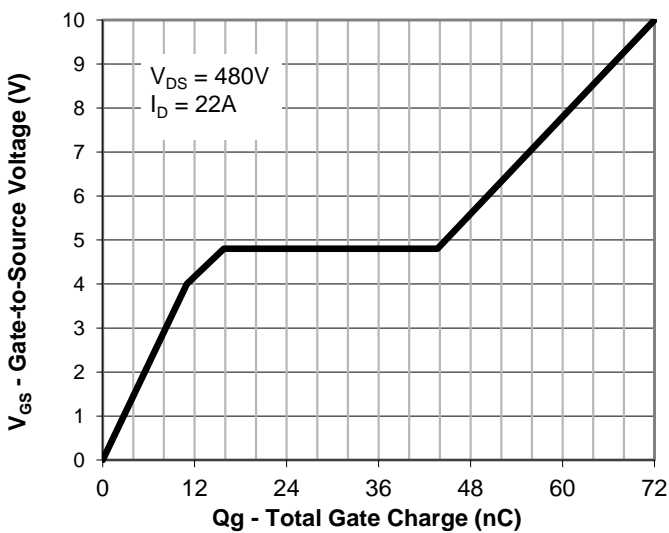
**On Resistance vs Junction Temperature**



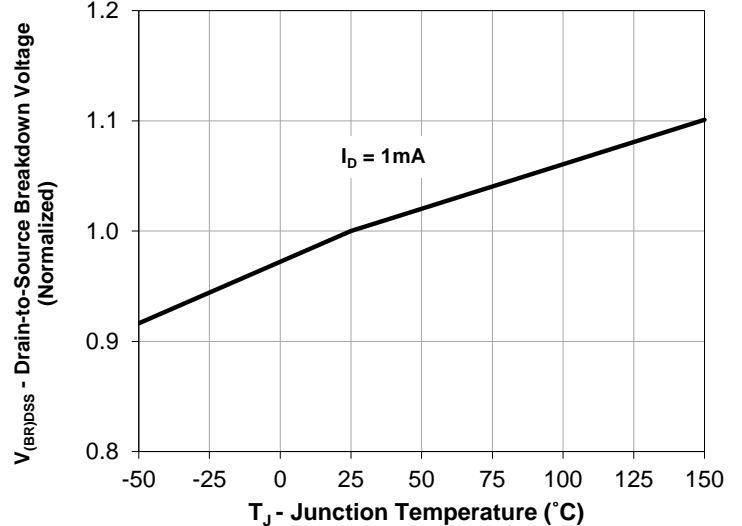
**Gate Threshold Voltage vs Junction Temperature**



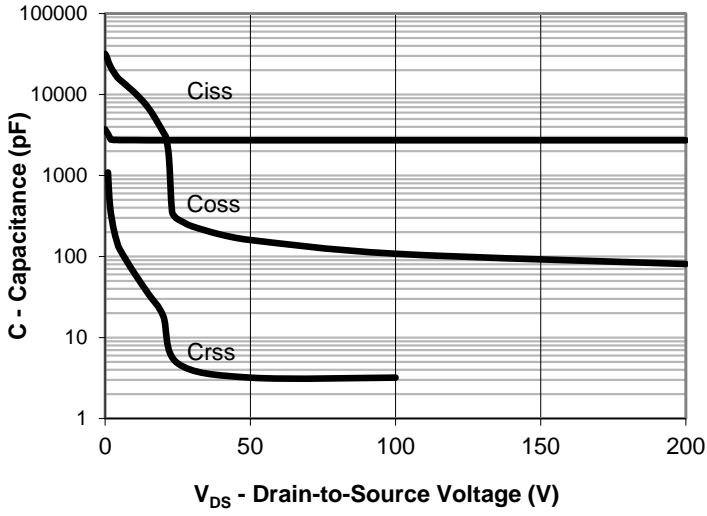
**Gate Charge**



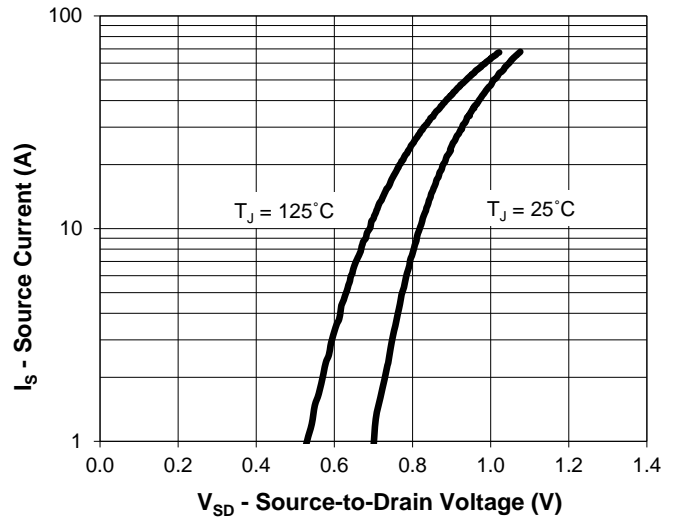
**Drain-to-Source Breakdown Voltage vs. Junction Temperature**



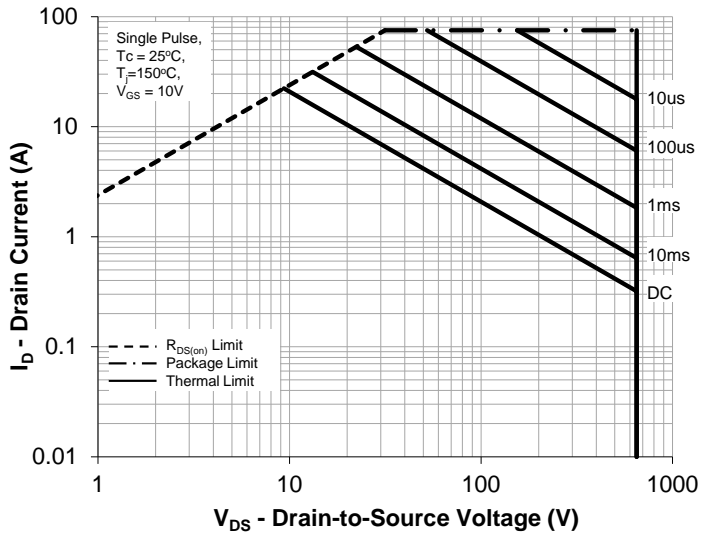
### Capacitance



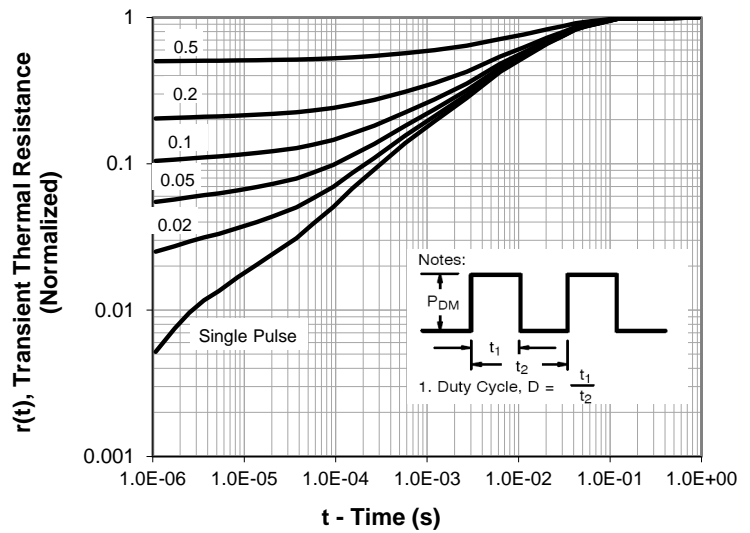
### Source-Drain Diode Forward Voltage



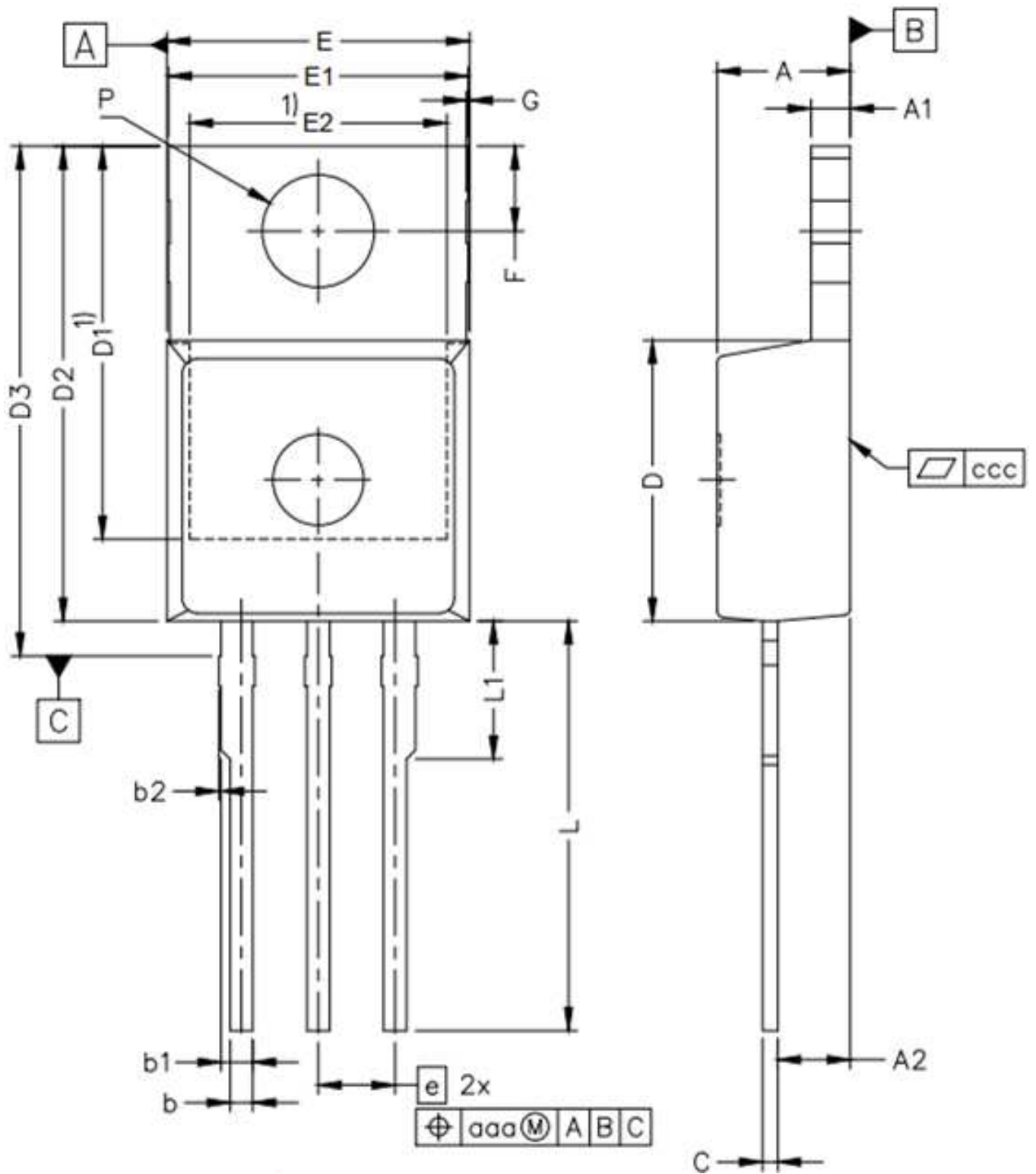
### Maximum Rated Forward Biased Safe Operating Area



### Transient Thermal Response, Junction-to-Case



Package Outline: TO-220



**NOTE :**

- 1). TYPICAL METAL SURFACE Min. X=7.25 / Y=12.3  
ALL METAL SURFACES: TIN PLATED, EXCEPT AREA OF CUT
2. DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS.  
ANGLES ARE IN DEGREES.
4. RADIUS ON TERMINAL IS OPTIONAL.
5. GENERAL TOLERANCES - LINEAR  $\pm 0.05$
6. PLASTIC BODY ANGLES: 5° UNLESS OTHERWISE SPECIFIED.
7. PLASTIC BODY RADIUS: MAX. 0.25 UNLESS OTHERWISE SPECIFIED.
8. PLASTIC BODY FINISHIN: MATT FINISHING Ra=1.7~2 MICRONS
9. MISMATCH MAX.=0.05 (CAVITY TO HOLE AXIS)}
10. ASTERISKED QUOTES ARE SUBJECTED TO THE SPC CALCULATION (Cp,K,Cpk).

SYMBOL	MIN	MAX
A	4.20	4.60
A1	1.20	1.40
A2	2.20	2.60
b	0.65	0.85
b1	0.95	1.15
b2	-	0.15
C	0.40	0.60
D	9.05	9.45
D1	12.95 REF.	
D2	15.35	15.95
D3	16.50	17.10
E	9.80	10.20
E1	9.70	10.10
E2	8.50 REF.	
e	2.54 BSC	
F	2.60	3.00
G	0.10 REF.	
L	13.00	14.00
L1	4.35	4.75
P	3.55	3.85
aaa	0.25	
ccc	0.05	

## **ICEMOS SUPERJUNCTION PATENT PORTFOLIO**

### **ICEMOS GRANTED PATENTS**

**US7,429,772**

**US7,439,178**

**US7,446,018**

**US7,579,607**

**US7,723,172**

**US7,795,045**

**US7,846,821**

**US7,944,018**

**US8,012,806**

**US8,030,133**

### **3D SEMI PATENTS LICENSED TO ICEMOS**

**US7,041,560B2**

**US7,023,069B2**

**US7,364,994**

**US7,227,197B2**

**US7,304,944B2**

**US7,052,982B2**

**US7,339,252**

**US7,410,891**

**US7,439,583**

**US7,227,197B2**

**US6,635,906**

**US6,936,867**

**US7,015,104**

**US9,109,110**

**US7,271,067**

**US7,354,818**

**US7,052,982,**

**US7,199,006B2**

Note: additional patents in China, Korea, Japan, Taiwan, Europe have also been granted to IceMOS and 3D Semi for Superjunction MOSFETs with 70 additional Patent applications in process in the USA and the above listed countries.



## Marking Information

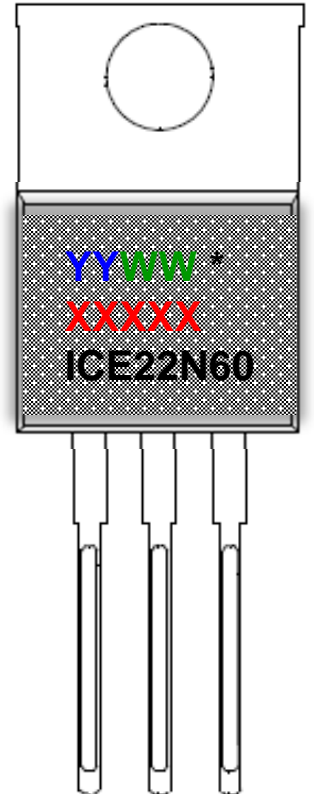
**YY** = Last two digits of the year

**WW** = Work week

**\*** = Site ID

**XXXXX** = Lot ID

**ICE22N60** = ICE is IceMOS logo and 22N60 is a designated device part number



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